A Segmented DAC based Sigma-Delta ADC by Employing DWA

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Abstract

Data weighted averaging algorithm work well for relatively low quantization levels , it begin to present significant problems when internal quantization levels are extended farther. Each additional bit of internal quantization causes an exponential increase in the complexity, size, and power dissipation of the DWA logic and DAC. This is because DWA algorithms work with unit-element DACs. The DAC must have $2^N - 1$ elements (where N is the number of bits of internal quantization), and the DWA logic must deal with the control signals feeding those $2^N - 1$ unit elements. This paper discusses the prospect of using a segmented feedback path with coarse and fine signals to reduce DWA complexity for modulators with large internal quantizers. However, it also creates additional problems. mathematical analysis of the problems involved with segmenting the digital word in a $\sum\Delta$ ADC feedback path are presented, along with a potential solution that uses frequency-shapes this mismatch error. A potential circuit design for the frequency-shaping method is presented in detail. Mathematical analysis and behavioral simulation results are presented.

Keywords : Sigma-Delta modulator, Data Weighted Averaging (DWA), Segmentation.

1 Introduction

The sigma-delta analog to digital converter ($\sum\Delta ADC$) has been widely used in recent decades for low frequency, high resolution (even up to 24 bit) applications such as digital audio and high-precision instrumentation [2], [8] Recent work, however, is extending the signal bandwidths of $\sum\Delta$ ADCs into the MHz range while maintaining high resolution [5].

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There are three ways to increase the resolution of $\sum\Delta$ modulators. one can increase the sampling frequency relative to the bandwith of interest, the order of the noise transfer function, and the number of internal quantization levels. All three of these approaches come with an attendant cost in power dissipation, the complexity and circuit area. Early $\sum\Delta$ converter used a single bit quantizer in the loop[3] , [4] because of their suitability for VLSI implementation and their superior linearity. The use of multibit quantization has been limited because non linearity in the DAC of a sigma-delta modulator translates directly into non linearity of the entire modulator, producing a distorted output. Non linearity in the DAC also modulates the quantization noise into the signal band, thus degrading the SNR. However, multibit modulators have several advantages such as increased resolution for the same oversampling ratio, improved stability, relaxed amplifier requirements and better tone behaviour. Attempts to eliminate the non linearity problem associated with multibit $\sum\Delta$ modulators have resulted in the use of DWA techniques which shape the noise generated by DAC unit element mismatch, shifting it to higher frequencies which are out of the band of interest.

Increasing internal quantization levels beyond five bits improves SNR but presents significant challenges. Both the internal quantizer and the DWA logic grow exponentially incomplexity, size, and power dissipation as the internal quantizer resolution increases.

Using a coarse/fine ADC is a logical alternative for reducing quantizer power. A folding ADC could provide quantization above eight bits while still maintaining the low latency required of the internal quantizer. Recent work has also shown that it is possible to incorporate two-step ADCs with in asingle loop modulator, permitting lower power quantizers while maintaining loop stability .[12],[13]

This paper will present an architecture that permit the uses of DWA with a coarse/fine quantizer. The paper is organized as fallow. In section 2, reviewes data weighted averaging technique for modulators $\sum\Delta$ ADC. In section 3, the proposed method of segmentation is described. In section 4, the problem segmented coarse/fine DAC structure is discussed. In section 5, method requantization to overcome this problem is presented. simulation results are shown to demonstrate this methods performance.

2 DWA Algorithm

Multi bit quantization improves the stability and the signal-to quantization noise performance of sigma-delta converters, but it necessitates the use of dynamic element matching (DEM) to filter the nonlinearity error in the signal band . Data weighted averaging (DWA) is the most widely used DEM algorithm, due to its simplicity and low hardware overhead.

The basic concept of DWA is to guarantee that each of the elements is used with equal probability for each digital input code. This is realized by sequentially selecting elements, beginning with the next available unused element. The operation principle is illustrated in Figure 1. v(n) denotes the DAC input at clock cycle n. In the 1st clock four unit elements are selected. Then in the next clock the elements are selected from the first unused, that is the 5th element. If the last element is selected, DWA will start to select the 1st one again. DWA shapes the nonlinear errors with the

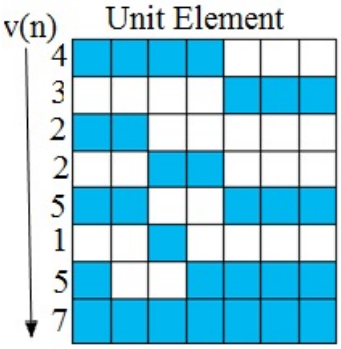


Figure 1: The DWA operation principle.

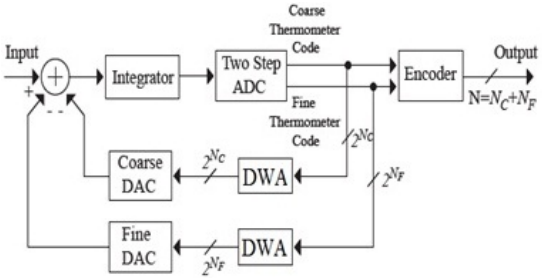


Figure 2: Block Diagram of Segmentated $\sum \Delta$ ADC.

first-order transfer function $(1 - z^{-1})$.[7]

3 DWA with Segmented Quantizer

A folding or two-step architecture for the internal quantizer can solve some of the problems arising from increasing the internal quantization level beyond 5 bits. Since these architectures provide the digital data in two sections, coarse bits and fine bits, a logical way to interface with the DWA is to simply perform DWA independently on the coarse and fine DAC banks, as illustrated in Figure 2.

The quantizer produces N_C bits as the coarse signal and NF bits as the fine signal, for a total of N bits $N = N_C + N_F$. Figure 3 shows a mathematical representation of the segmented architecture from Figure 2.

The two-step quantizer resolves the N_C coarse bits, and then subtracts this value from the input and generates the N_F fine bits from this signal. The gain of $2^{-(N-N_C)}$inside the quantizer represents a binary right shift to insure the correct place value of the bits, since the coarse bits are the NC most significant bits of an N bit signal. Since DWA shapes the error due mismatch unit element DAC

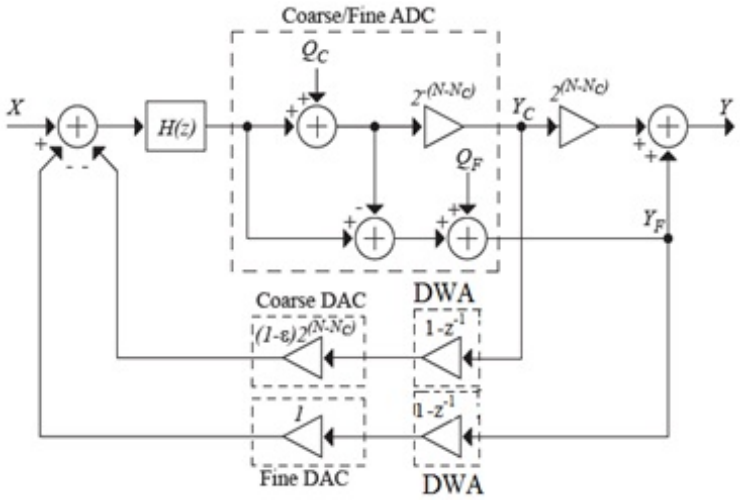


Figure 3: Mathematical Block Diagram of Segmented $\sum \Delta$ ADC.

with first order transfer function , the DWA blocks can be represented as $(1-z^{-1})$, as seen in Figure 3. The coarse and fine outputs are each applied to separate DACs using smaller, independent DWA circuits, reducing DWA complexity significantly. The coarse DAC transfer function is weighted by $2^{(N-N_C)}$ times that of the fine DAC to insure that the original place values are preserved. However, since this weighting depends on the size of the unit elements involved, a gain mismatch, $1-\epsilon$, will be present. The quantization noise, Q_C, present in both signals Y_c and Y_F , ideally will cancel when the coarse and fine signals are summed together at the modulator input. This result should be the same as if a single DWA circuit with a single DAC had been in the feedback path. However, because of the gain mismatch between the DACs, the coarse quantization error will not completely cancel and will be transmitted to the output.

4 Analysis of the problem DWA

when the coarse and fine signals are summed together, the quantization noise will not completely cancel while in the non segmented (single-path) case would completely cancel Because of gain mismatch between the coarse and fine DAC banks in the segmented case. The non-canceled portion of the quantization noise will be added directly to the input signal, and thus be transmitted to the output of the ADC. The output, Y, of the ADC in Figure 3 can be written as :

$$Y(z) = Y_C(z).2^{N-N_C} + Y_F(z) \tag{1}$$

where

$$Y_C(z) = \frac{2^{-(N-N_C)}.(Q_C(z) + (X(z) - (1-z^{-1})Y_F(z)H(z))}{1 + (1-\epsilon).(1-z^{-1}).H(z)} \tag{2}$$

and

$$Y_F(z) = -Q_C(z) + Q_F(z) \tag{3}$$

by substituting equation 2 and equation 3 into equation1, it is obtained as follows :

$$Y(z) = \frac{X(z).H(z)}{1 + (1-\epsilon).(1-z^{-1}).H(z)} + \frac{Q_F(z)}{1 + (1-\epsilon).(1-z^{-1}).H(z)} + \frac{\epsilon.(1-z^{-1}).(Q_C(z) - Q_F(z))}{1 + (1-\epsilon).(1-z^{-1}).H(z)} \tag{4}$$

For comparison, a non-segmented (single-path) approach would lead to:

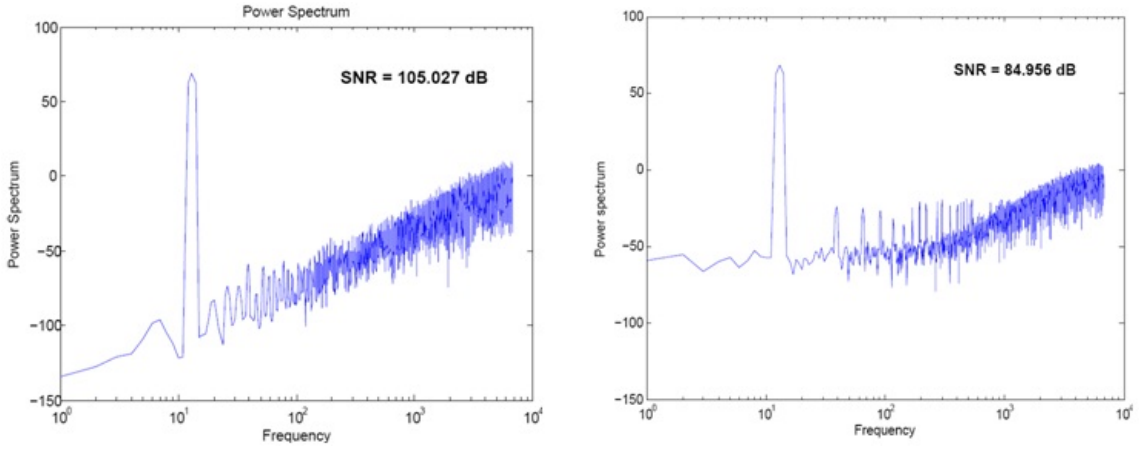
$$Y(z) = \frac{X(z).H(z)}{1 + (1-z^{-1}).H(z)} + \frac{Q(z)}{1 + (1-z^{-1}).H(z)} \tag{5}$$

A comparison of equation 4 and equation 5 shows that the segmented system has the error term $\epsilon.(Q_C - Q_F).(1-z^{-1})$ present in addition to normal quantization noise. The value of the mismatch term, , changes with each clock cycle due to the operation of the DWA. For realistic unit-element mismatch values, is small, but still large enough to significantly affect the SNR of the system. Figure 4 shows the output spectrum for both non segmented and segmented systems for a second order modulator with an OSR of 32 and 1% element mismatch. the non segmentation represents a DAC with 8-bit DWA. For the segmentation system and 1% mismatch, using independent coarse/fine DWA results in a 20 dB degradation in SNR from the non segmented case.

5 The Noise Shaped Requantization Metode

The mismatch error between coarse and fine banks can be noise shaped if the coarse quantization is performed within a digital $\sum\Delta$ modulator. This method was initially proposed in [16] for a $\sum\Delta$ DAC, then this method in[15] was proposed for $\sum\Delta$ ADC along DEM with gain of unity. This extends this concept to $\sum\Delta$ ADCs with DWA algorithms.The basic idea is work to generate a new coarse signal with a digital $\sum\Delta$ modulator and use this coarse signal to generate a new fine signal. This insures that both the coarse and fine signals are individually noise shaped, which is performed in a way that causes the quantization error leakage to be noise shaped as well. Even though it does not completely cancel errors due to DAC mismatch, the quantization error noise power will be outside the signal band. The process is modeled in Figure 5. Figure 6 shows a mathematical representation of the ReQ architecture from Figure 5. The digital coarse and fine signals from the quantizer are first concatenated to form an N-bit signal. This signal is then requantized to NC bits using a digital first-order $\sum\Delta$ modulator. Then coarse signal is subtracted from the original N-bit signal to form the new fine signal, comprised of $N_F + 1$ bits. After requantization, the new coarse and fine signals become:

$$Y'_C(z) = 2^{-(N-N_C)}.(Y(z) + Q'_C(z).(1-z^{-1})) \tag{6}$$



(a) non segmentation (b) segmentation

Figure 4: Output spectrum of the $\sum\Delta$ modulator employing (a)non segmentation and (b)segmentation.

$$Y'_F(z) = -Q'_C(z).(1 - z^{-1}) \tag{7}$$

Signals $Y'_C(z)$ and $Y'_F(z)$ then pass through independent DWA blocks and DACs and are summed at the input of the modulator. With first-order requantization (ReQ), the quantization error that is not completely cancelled due to coarse/fine DAC mismatch as in equation 4 is noise-shaped away from the signal band. The output of the system with ReQ as in Figure 6 is derived as follows:

$$Y'(z) = Y_C(z).2^{N-N_C} + Y_F(z) \tag{8}$$

where

$$Y_C(z) = 2^{-(N-N_C)}.(Q'_C(z) + X(z) - (1-\epsilon).(1-z^{-1}).2^{(N-N_C)}.Y'C(z) - Y'F(z)(1-z^{-1})H(z)) \tag{9}$$

and

$$Y_F(z) = Q'_C(z) + Q_F(z) \tag{10}$$

by substituting equation 9 and equation 10 in to equation 8, it is obtained as follow:

$$Y'(z) = \frac{X(z).H(z)}{1 + (1-\epsilon).(1-z^{-1}).H(z)} + \frac{Q_F(z)}{1 + (1-\epsilon).(1-z^{-1}).H(z)} + \frac{(\epsilon.Q'_C(z))(1-z^{-1})^2.H(z)}{1 + (1-\epsilon).(1-z^{-1}).H(z)} \tag{11}$$

which shows that that the coarse quantization noise leakage is first-order shaped. Figure 7 shows the output spectrum for ReQ method. again 8bit two-step quantizer, second order modulator with OSR of 32 was used.Table 1 shows simulated results. First row is the SNR of non segmented $\sum\Delta$

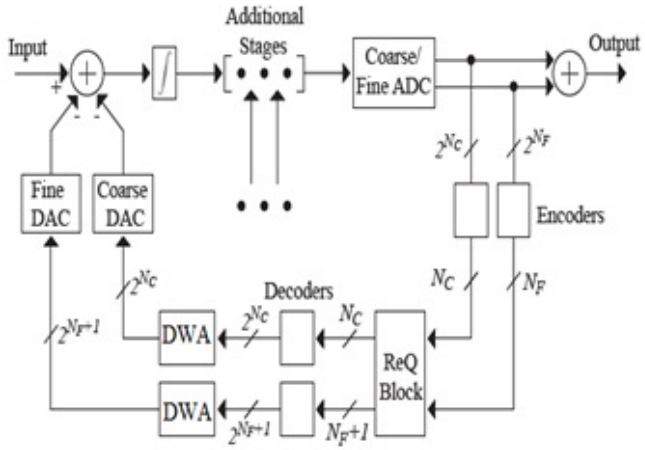


Figure 5: Block Diagram for ReQ Metode.

ADC at various unit-element mismatch values. The second row shows the segmented case. The third row shows the ReQ case. At 1% mismatch, the segmented ADC has an SNR 20 dB lower than the non-segmented case. In comparison, the ADC with ReQ has an SNR only 2 dB lower than the non segmentated case.

Table 1: Simulated result

Methods	Unit Element 0% Mismatch	Unit Element 0.5% Mismatche	Unit Element 1% Mismatch
Non segmented	106.7	106.21	105.027
segmented	106.7	90.02	84.956
ReQ	106.7	105.12	103.64

6 Conclusion

The DWA algorithm modulates the nonlinarity of the DAC due to mismatch unit element, moving the harmonic distortion out of the signal bandwidth, which can be removed by the digital low-pass filter in the following stage. However each added bit of quantizer casuses an exponential increase in complexity of DWA and DAC circuitry. A segmented architecture with coarse/fine DAC and DWA combined with the ReQ method has been proposed to reduce the complexity of DWA and DAC due to the large number of bits used in the internal quantization.The ReQ method proposed in this paper allow for larger internal quantizers without the exponential increase in DWA and DAC circuits,while still maintaining performance close to the one quantizer with DWA system.

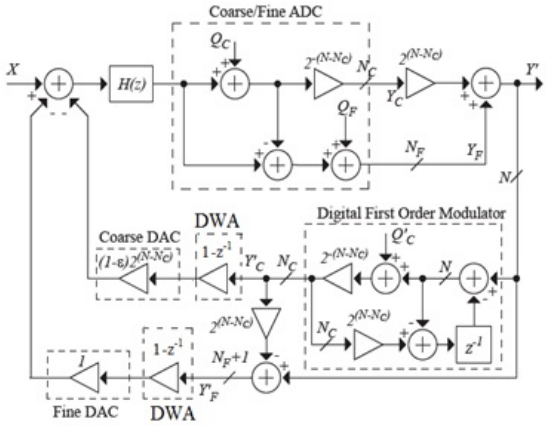


Figure 6: Mathamatical Block Diagram of ReQ Metode.

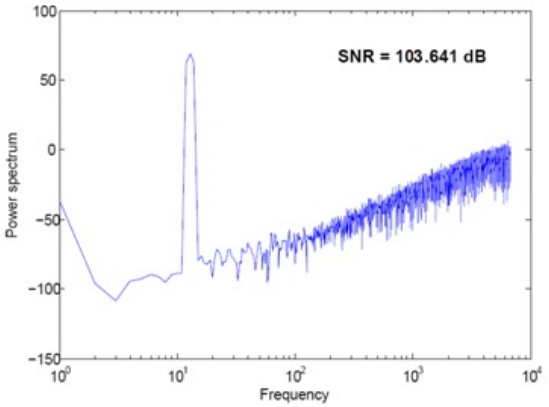


Figure 7: Output Spectrum the $\sum \Delta$ modulator using method requantization.

References

[1] A. A. Hamoui and K. W. Martin. High-order multibit modulators and pseudo dataweighted-averaging in low-oversampling AS ADCs for broad-band applications. *IEEE Trans. Circuits Syst. I*, 51:72–85, 2004.

[2] I. Galton. Why Dynamic-Element-Matching DACs Work. *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2:69–74, 2010.

[3] R. Koch, B. Heise, F. Eckbauer, E. Engelhardt, J. A. Fisher, and F. Parzefal. A 12-bit sigma-delta analog-to-digital converter with a 15-MHz clock rate. *IEEE Trans. Circuits Syst. I*, 21:1003–1010, 1986.

[4] M. Rebeschini, N. R. van Bavel, P. Rakers, R. Greene, J. Caldwell, and J. R. Haug. A 16-b 160-kHz CMOS A/D converter using sigma-delta modulation. *IEEE Trans. Circuits Syst*, vol. 25,:431–440, 1990.

[5] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen. A 3.3-V, 15-bit, Delta-Sigma ADC With a Signal Bandwidth of 1.1 MHz for ADSL Applications. *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7:927–936, 1999.

[6] I. Fujimori, A. Nogi, and T. Sugimoto. A multibit delta-sigma audio DAC With 120dB dynamic range. *IEEE Journal of Solid-State Circuits*, vol. 35,:1066–1073, 2000.

[7] R. T. Baud and T. S. Fiez. Linearity Enhancement of Multibit AID and D/A Converters Using Data Weighted Averaging. *IEEE Trans. Circuits Sysl.*, vol 42 :753–762, 1995.

[8] S. R. Norsworthy, R. Schreier, and G.C. Temes Delta-Sigma Data Converters. *IEEE Press*, 1997.

[9] D. H. Lee and T. H. Kuo. Advancing data weighted averaging technique for multi-bit sigma-delta. *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 54,:838–842, 2007.

[10] Alex Jianzhong Chen, Member, and Yong Ping Xu, Senior Member. Multibit Delta-Sigma Modulator with Noise-Shaping Dynamic Element Matching. *IEEE Trans. Circuits Sysl.*, vol 56 :1125–1133, 2009.

[11] Nevena Rakuljic, Member, and Ian Galton, Senior Member TreeStructured DEM DACs with Arbitrary Numbers of Levels. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMSI*, vol. 48,:313–322, 2010.

[12] S. Lindfors and K. A. I. Halonen Two-step Quantization in Multibit Delta-Sigma Modulators. *IEEE Trans. Circuits Sysl.*, vol 48 :171–176, 2001.

[13] Y. Cheng, C. Petrie and B. Nordick. A 4th-Order Single- Loop Delta-Sigma ADC with 8-Bit Two-Step Flash Quantization. *submitted to Proc. ISCAS 2004*, 2004.

[14] A. Fishov, E. Siragusa, J. Welz, E. Fogleman, and I. Galton. Segmented Mismatch-Shaping D/A Conversion. *2002 IEEE International Symposium on Circuits and Systems (ISCAS).*, vol 4 :679–682, 2002.

[15] Brent Nordic, Craig Petrie, and Yongjie Cheng. Dynamic Element Matching Techniques For Delta-Sigma ADCS With Large Internal Quantizers. *submitted to Proc. ISCAS 2004*, 2004.

[16] R. Adams, K. Nguyen, and K. Sweetland. A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling. *IEEE Journal of Solid-State Circuits.* 1871–1878, 1998.