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Behavior Model of Noise Phase in a Phase Locked Loop Employing Sigma Delta Modulator

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Abstract. This paper proposes two techniques for fractional-N synthesizers to cancel the quantization noise and spurs. This technique has advantages over the dynamic element matching (DEM), also for recovering the input rising edges signals during the reset and improving the frequency effect, delay elements (Des) is inserted in the input and feedback signal paths of PFDs. Simulation results, has been performed to validate the claim.

Keywords: Fractional-N, noise cancellation, spurs, delay elements.

1 Introduction

Frequency synthesizers are the heart of each transmitter/receiver system. Almost every communications consumer product employs a frequency synthesizer often operating as a local oscillator providing the carrier frequency of interest. Mobile phones, radios, and televisions are a few among the many applications that incorporate frequency synthesizers.

At its simplest, an Integer-N PLL fails to achieve wide tenability and fine resolution as it is limited by integer multiples (N) of a fixed crystal frequency. Additionally, its phase noise performance is degraded due to large value of N. Fractional-N PLLs, can solve this limitation by allowing for fractional multiplication

of reference frequency, by enabling the use of a high-frequency reference signal and much lower division values while still maintaining the required resolution.

In this paper, two techniques are applied to reduce the previous problems. To achieve second order mismatch shaping, without DEM and thermometer coded, a second order binary weighted D/A differentiator (DAD) is used. In addition, delay elements (DEs) in the input and feedback signal paths of the PFDs is inserted to recover the input signal rising edges arriving during the reset and reduce the frequency effect.

The rest of the paper is organized as follow: section II and III and IV describes the architecture of second order binary-weighted DAD and its unique advantages. Section V and VI describe linearization of PFD and effected it on phase noise. Section VII shows simulation results. Finally, section VIII concludes the paper.

2 Noise Cancelation

In general, the characteristic of quantization noise must be randomized but in practice has definite. This problem can be solved by integrating the deference between I/O of the ∑Δ modulator [9] and sum it with inversed signal through a DAC at output of CP. However these methods as well as other noise cancelation methods have two limits [12]: 1- A large-bit width high order ∑Δ modulator needs for fractional-N PLL to give fine frequency resolution and fast locking time. But, to reduce complexity of the DAC, second quantizer must be used to reduce the input bits of it. Under this conditions, extra quantization noise, through second quantizer, add to the PLL [12]. To eliminate this noise, another ∑Δ modulator is needed to shape it. This method appear to reduce the noise quantization but at the high cost of increasing the hardware [12]. 2- This mismatch of DACs elements adds extra phase noise to the circuit. To solve this problem, DEM methods is used to convert these mismatches to the white noise [1] [12]. The drawbacks of this method are high power dissipation of DSP and increase the area of circuit. Another method such as DAC full-segmented also is used, but doubles DACs units and increase hardware [12].

3 Mash Structure

The MASH architectures [10][11] have the simplest configuration, because they only required adders and registers to be implemented. The MASH modulation uses accumulators in a cascade configuration, the quantized output of each stage is processed by noise cancellation logic, Fig. 1. Since, for digital MASH architectures, the noise cancellation logic is perfect, the quantization noise is only that of the last accumulator (with a shaping order equal tothe modulator's order).

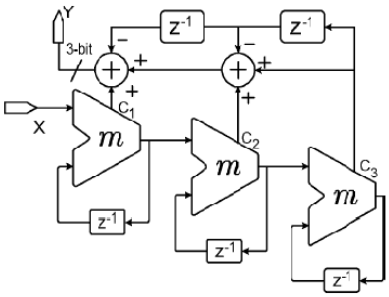

Fig. 1. Digital mash sigma delta modulator[12]

This architecture is inherently stable and the dynamic range consists of all the input quantization level. Moreover, the noise transfer function has the same high-frequency behavior as same multi loop architectures. Also, MASH 1-1-1 has the advantage of tapping out the unprocessed quantization error, Fig. 2 [12] and generation a cancellation signal from the unprocessed quantization error is much simpler. The previous methods needed 6 bit quantizer to limit the number of DAC's bit, 3 sequential differentiators to achieve noise cancellation signal e $(1-z^{-1})^3$ and high pass filter the second quantization noise, e_2. But this method does not require any of these [12].

The second order binary-weighted D/A differentiator was fully described in [12] and in this work, we will refer to it. The binary weighted D/A differentiator usually

was used for Sigma-Delta D/A converters [12].

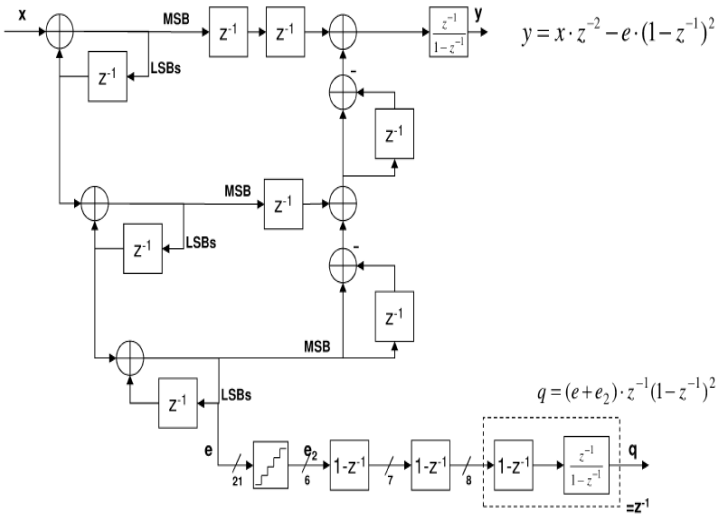

Fig. 2. Cancelation by MASH1-1[12]

It is also suitable for cancelling the quantization noise in Fractional-N PLLs. The output of the DAD with binary weighted is a second order high-pass shaping function to multi-bit DAC mismatch without need to DSP [12]. Second order DAD can be implemented with four DAC elements in two stage cascaded differentiators to realize the $(1-z^{-1})^2$ function, as shown in Fig. 3 [12]. The mismatch from each DAC element is assumed to be a, b, a_2 and b_2, respectively[12]. As the signal swaps every other clock cycle at the first stage output, $p_1(n)$ and $p_2(n)$ will from complementary pairs. Subsequently, the only possible values at outputs of second stage differentiators, $[(p_1(n), -p_1(n+1)]$ and $[p_2(n), -p_2(n+1)]$, are either [(0,1), (1,0)] or [(1,0), (0,1)] [12]. Therefore, the errors at the output of the left DAC pair can only be [(0,a), (b,0)] or [(a,0), (0,b)]. Taking discrete Fourier transform of these sequences, the sum output noise at the left half of the second order DAC becomes [12]. If the mismatch between two DAC elements is identical, a=b, a second order shaping function can be achieved [12].

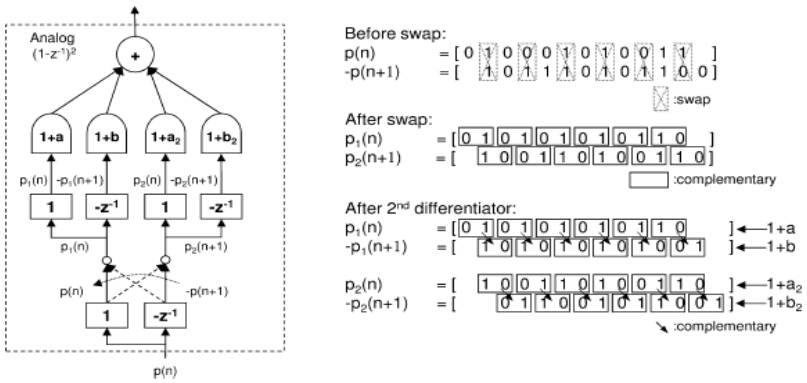

Fig. 3. Shaping using second order DAD[12]

Similar expressions can be derived for the right half of second order DAD. According to (3), as long as the differential mismatch between adjacent elements is minimized, second order mismatch shaping can be realized [12]. Consequently, the stringent requirement on the global matching of a traditional multi-bit DAC can be relaxed to the local matching between adjacent DAC elements [12]. This can be easily accomplished by routing symmetric adjacent with inter-digitated structure to minimize the process mismatch [12].

The multi-bit DAD can also be implemented with binary-weighted architecture without suffering from large differential non-linearity (DNL) in Fig. 4[12]. It is because gain error in each binary-weighted DAD element can be traded as the common-mode mismatch and filtered by second order high-pass function. There are three advantages of second order binary-weighted DAD over first order thermometer-code or fully-segmented DAC with DEM [12]. First, the second order orcommon mode mismatch shaping can tolerate bigger mismatch due to process variation and routing parasitic. In fact, it offers 20dB more reduction in simulation with the same mismatch condition [12]. Second, the DAD implementation does not require DSP power compared to DEM implementations. Finally, the binary weighted DAD uses less DAC elements than a thermometer-coded DAC and it occupies half the area of a fully-segmented DAC[12].

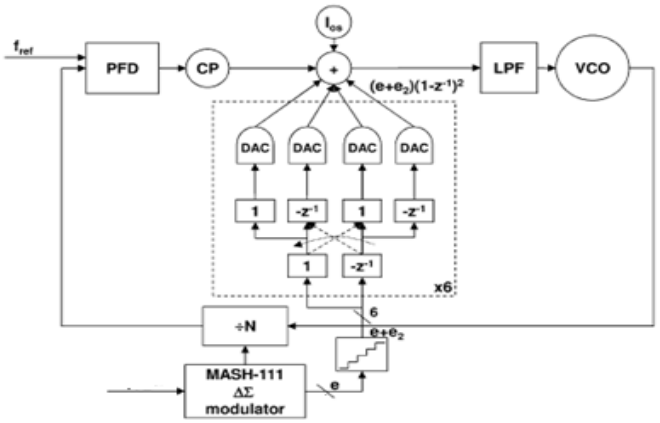

Fig. 4. Second order binary-weighted DAD in fractional-N PLL [12]

4 Linearization

The phase/frequency detector with charge pump (PFD/CP) is a sequential phase detector with the ability of also locking the frequency that is mostly used for implementation of fractional-N PLLs, Fig. 5.

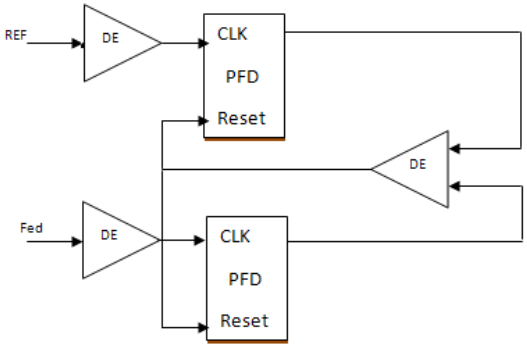

Fig. 5. Proposed PFD

This type of phase/frequency detector, despite the most used in implementation of locked loops [13], presents non-ideal effects that degrade the PLL overall performance, as a consequence of a modulation in the VCO line of control, the most important of this problems is dead zone. This dead zone provides the rising of the jitter at the output of the loop that is an increase in phase noise of the PLL. In this work used an even number of inverters in the reset of the PFD flip-flops that do not change its logic state, but give rise to a delay in the signal large enough to cancel it. Also in this work used a continues-time linear model for sequential-type PFD [14]. In this model used delays in inputs of DFFs of the PFD. With this methods a frequency gate delays is derived. Fig. 6 shows the normalized PFD output up-dn as a function of phase difference between the two inputs. The mathematical expression of this method was presented in [14].

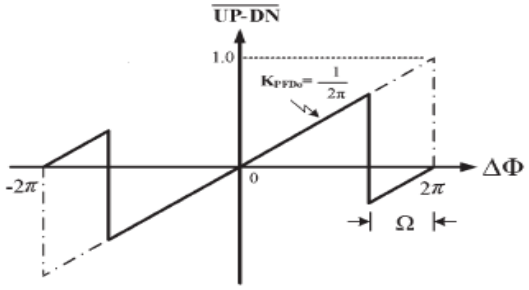

Fig. 6. Normalized PFD output[14]

5 Estimation of Delay

The most important aspect of the design of this paper is without doubt the estimation of delay used in the PFD. The minimum delay that must be introduced in the reset path has been estimated as the average value of the time it takes the pulses in the output nodes up and dn to rise and fall [15]. The minimum CP on-time τ_d is

introduced by feedback delay circuit. The propagation delay from the reset input to the output of the DFF is τ_p. In Fig. 7 [15], τ_p^h and τ_p^l respectively, present the DFF reset propagation delay for high and low clock input levels. $\tau_{FB}$is the pulse width of FB signal, for the case that FB is lead (Fig()). DE is the delay that introduce in the input of the DFFs[14]. For case that FB is lead the pure on-time of CP is given by[15]. It can be observed that un-equal propagation delay result in an offset from the ideal on-time of the CP given by δ_k. On the other hand when the FB pulse is lag fig(7). Both signals (FB and REF) are high when reset goes active. The pure on-time of CP is given by[15]. In this case the CP on-time is correct. In [15] a statistical method is used to determine the PSD noise due to reset delay mismatch in the PFD.

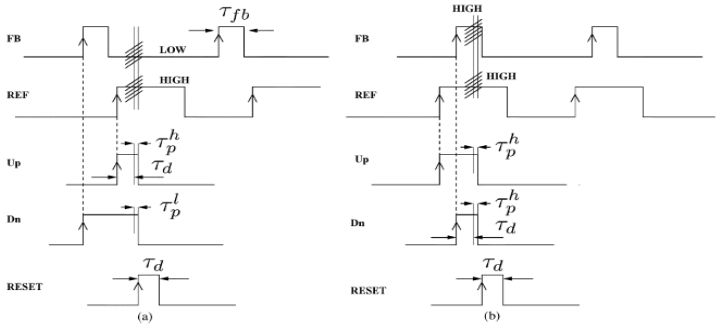

Fig. 7. Reset delay mismatch (a) Early FB pulse (b) late FB pulse [15]Shaping

6 Simulation Results

The simulation result of fractional-N PLL based on proposed method was simulated in Simulink Matlab and Matlab code. Included is the design of fully integrated 1.74GHz ∑Δ-Fractional-N PLL frequency synthesizer. It takes advantage of a ∑Δ modulator to get a very fine frequency resolution and relatively large loop bandwidth. This frequency synthesizer is a forth order charge pump PLL with 40MHz reference frequency. The loop band-with is about 100KHz, Fig. 8 shows complete block diagram of the proposed fractional-N synthesizer. Fig. 9 shows the

phase noise of the output of the PLL, we can see that the phase noise of the output is about -90dB at 1MHz offset frequency. Fig. 10 shows the output spectrum, we can see in the output spectrum, the spur tone was eliminated.

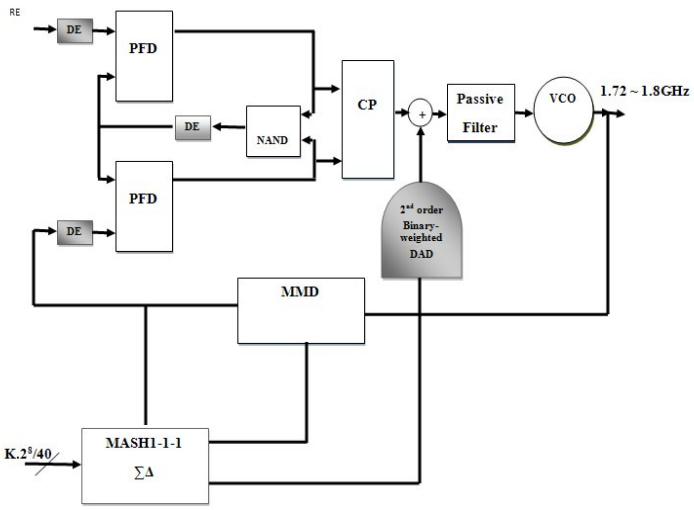

Fig. 8. Complete block diagram of proposed fractional-N synthesizer

7 Conclusion

A fractional-N frequency synthesizer based on ∑Δ is presented. In this work, two techniques are applied to cancel quantization noise and spurs. First, it was used a ∑Δ-modulator with second order binary-weighted (DAD) to achieve second order mismatch shaping. Secondly, used delay elements (Des) in the input and feedback signal paths of PFD to recover the input rising edges signals during the rest and improve the frequency effect. With these methods, quantization noise and spurs are eliminated,it also reduced the number of elements and the circuit is compacted over

the previous methods like DEM.

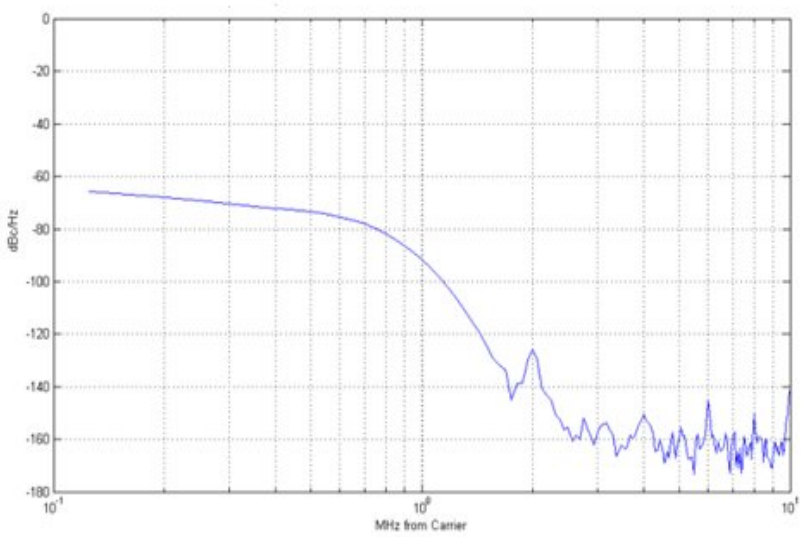

Fig. 9. Phase noise of the output

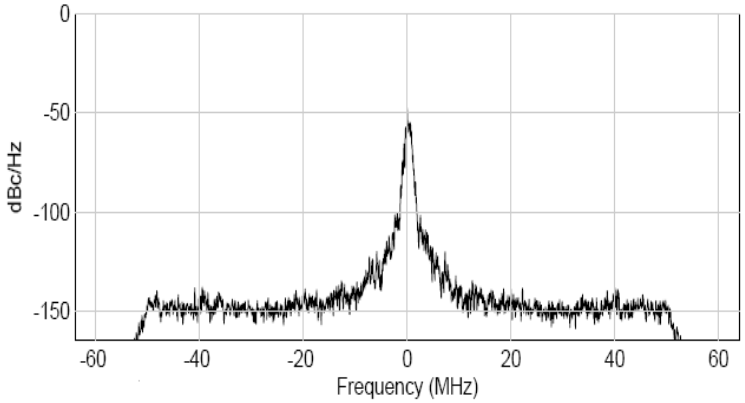

Fig. 10. Spectrum output

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