

A Semi-Analytical Drain Current Deflection Model for the Symmetric Pocket Implanted n-MOSFET Using Lorentz Force Analysis

Muhibul Haque Bhuyan¹, Fouzia Ferdous² and Quazi D M Khosru³

¹Department of Electrical and Electronic Engineering,
Green University of Bangladesh, Mirpur 2, Dhaka, Bangladesh.

²Department of Electrical and Electronic Engineering,
International Islamic University Chittagong, Dhanmondi, Dhaka, Bangladesh

³Department of Electrical and Electronic Engineering,
Bangladesh University of Engineering and Technology, Dhaka, Bangladesh
E-mail: muhibulhb@gmail.com, fferdous91@yahoo.com and qdmkhosru@eee.buet.ac.bd

Abstract. This paper introduces the effect of magnetic field upon the deflection of the subthreshold drain current of the symmetric pocket implanted n-MOSFET. The symmetric pocket implanted n-MOSFET's surface potential, threshold voltage, electron mobility and subthreshold drain current models are used to study the effect of magnetic field on the subthreshold drain current deflection in the inversion channel. Magnetic field strength is varied from ± 200 mT to ± 250 mT. Results verify the theoretical derivations. This model can be used if short channel n-MOSFETs are used to develop the Magnetic FET Sensors (MFS) that have many practical applications.

Keywords: Pocket Implanted n-MOSFET, Magnetic FET Sensor, Subthreshold Drain Current Deflection.

1 Introduction

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the main building block in the Integrated Circuit (IC) since its invention due to its low power consumption, high speed and low noise [1-4]. Therefore, many research works have been carried out for this device and novel MOSFET structures are being introduced to enhance device performance as well as device applications [5-11]. In the modern electronic systems design, electromagnetic compatibility (EMC) problem is a crucial factor. As the operating frequencies as well as the number of transistors integrated in the ICs increase, radiated and conducted electromagnetic emissions of ICs also

¹ The corresponding author.

increase due to the large current flow during a short period of time. Thus several measurement and testing techniques based on thin-film magnetic field, electro-optic or magneto-optic probes have been selected by regulatory committees as standard methods [12-16]. But all of these passive testing elements have a fundamental tradeoff between their sensitivity and spatial resolution as well as an incompatibility between spatial resolution and test efficiency. To solve these problems, an on-chip magnetic probe based on a magnetic field-sensitive Split-Drain MOSFET (MAGFET) that works as an active element was proposed. Many integrated magnetic sensor circuits use a MAGFET structure as a sensing element [17].

The MAGFET is a MOSFET with a single gate and two or more symmetrical drains sharing the total channel current. An imbalance between drain currents occurs due to the influence of a magnetic field. In spite of its large offset, temperature drift and noise, the MAGFET remains a popular magnetic field sensing device because of its easy integration with other electronic signal conditioning blocks in silicon chips. The list of magnetic sensor applications includes, but is not limited to, position-sensing, non-contact switching [18], vehicle detection [19], navigation [20], mineral prospecting [21], brain function mapping [22], contactless temperature measurement [23], wireless sensor network [24], earth magnetic field [25] etc. As an example, there can be as many as 40 magnetic field sensors in a modern automobile which are used for various purposes [19].

Designing a sensor is impossible without the device simulation tools which help to predict sensor behavior [26] before actual sensors are fabricated. Device simulation [27] has become very important, because, it is almost cheaper than performing experiments and provides insight into the internal physical mechanisms associated with device operation. Some efforts have been developed using numerical model such as finite element, Galerkin's residual method and finite difference scheme [28]. Other works propose a semi-analytic model [29-31] based on semiconductor physics and electromagnetic theory but it cannot be linked with circuit simulation tools. Another model based on empirical relation [32] does not reflect the physical behavior and geometrical effects of the device. Pocket implanted MOSFET is a good choice to combat Short Channel Effect (SCE). Many research works have already been conducted to develop drain current model of this device [6, 33-34]. Pocket profile has been modeled by different profiles [6, 35-37]. In this paper, a semi-analytical model that includes geometrical effects and linear pocket profiles on the subthreshold drain current deflection due to the presence of magnetic field has been developed.

2 Drain Current Deflection Model

The pocket implanted n-MOSFET structure shown in Fig. 1 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. Localized extra dopings are shown by circles near the source and drain sides. All the device dimensions are measured from the oxide-silicon interface. In the structure, the

junction depth (r_j) is 50 nm. The channel length (L) is 100 nm and width (W) is 500 nm, oxide thickness (t_{ox}) is 5 nm, and it is SiO₂ with fixed oxide charge density of 10¹¹ cm⁻². Uniformly doped p-type Si substrate is used with substrate doping concentration (N_{sub}) of 2×10¹⁷ cm⁻³ with pocket implantation both at the source and drain sides with peak pocket doping concentration (N_{pm}) of 2×10¹⁸ cm⁻³ and pocket length (L_p) of 50 nm. The n^+ source or drain doping concentration (N_{sd}) is 9.0×10²⁰ cm⁻³. The n^+ drain is split vertically with vertical distance of D_1 each and the gap between the two is d .

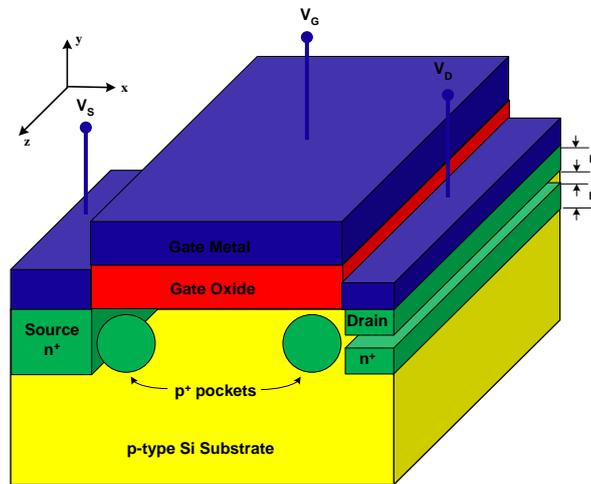


Fig. 1. Pocket implanted n-MOSFET structure with split drains.

The model of the conventional bulk n-MOSFET exhibits drastic reduction of the threshold voltage (V_{th}) having channel length in the sub-micron regime. This is known as Short Channel Effect (SCE). It has already been observed that by introducing Reverse Short Channel Effect (RSCE), SCE can be minimized [6]. In the case of RSCE, threshold voltage increases with decreasing channel lengths. This effect comes from the extra doping or pockets or fixed oxide charge located near the source and drain sides. Pocket implantation is done by adding extra impurity atoms (similar to that of the substrate) near the source and drain. This doping concentration is then caused to decrease from the source and drain sides towards the centre of the device along the channel. In [35], few simulated lateral pocket doping profiles are provided for different channel lengths after thermal annealing. After examining these pocket doping profiles, it is assumed that the pocket profiles to be linear and symmetric at both source and drain sides. It has been already shown that the linear profile can produce RSCE in threshold voltage model of the pocket implanted n-MOSFET [38]. This profile assumes that the peak pocket doping concentration decreases linearly to the substrate doping concentration with pocket lengths from both edges towards the center of the device along the channel [6].

These two conceptual pocket profiles are integrated mathematically along the channel from the source side to the drain side and then the integration result is divided by the channel length (L) to derive an average effective doping concentration (N_{eff}) as in equation (1).

$$N_{eff} = N_{sub} \left(1 - \frac{L_p}{L} \right) + \frac{N_{pm} L_p}{L} \quad (1)$$

This effective doping concentration expression has been used in deriving the several parameters of the device and then finally the drain current deflection model using Lorentz force analysis.

When a magnetic field is applied to a flow of charge carriers (for instance, electrons) moving through a quasi-straight path, they tend to move according to a non-linear trajectory [12]. The deflection of electrons under the magnetic field due to the Lorentz force can be calculated by solving the equation (2).

$$\vec{F}_m = q(\vec{v}_d \times \vec{B}) \quad (2)$$

From equation (2), it can be said that the higher the drift velocity the higher the magnetic force that produces larger deflection. It is known that the carrier deflection has been quantified using, as a measurement tool, the Hall Effect. This procedure has been used to measure the carrier deflection in extremely thin metallic plates that is commonly called Hall element. The inversion layer of a MOSFET can be used as a very thin hall element. However, to obtain a uniform structure, the inversion layer must be the channel of a MOSFET operating in the linear region, i.e. drain potential (V_{DS}) must be smaller than the gate overdrive voltage ($V_{GS} - V_{th}$), i.e. $V_{DS} \ll (V_{GS} - V_{th})$.

To describe how this MOSFET works, we propose a semi-analytical model based on semiconductor physics and electromagnetic theory. Few assumptions were taken into account [39]:

1. A uniform magnetic-field induction is applied perpendicularly to the gate plane only, and
2. The velocity of the ensemble of carriers along the channel is considered to have an average value v_d .

Additionally, the electric fields are labeled E_y and E_z , where the first/second component is the longitudinal/ perpendicular one. To quantify the electric field effect, we propose a model based upon Lorentz Force as in equation (3) and Newton's second law of motion. Starting by Lorentz force analysis, we obtain the force components (F_x , F_y and F_z) as in equation (8). With the presence of electric field, equation (2) can be written as in equation (3).

$$\bar{F}_m = q(\bar{E} + \bar{v}_d \times \bar{B}) \quad (3)$$

$$\bar{F}_m = \hat{i}F_x + \hat{j}F_y + \hat{k}F_z \quad (4)$$

$$\bar{E} = \hat{i}E_x + \hat{j}E_y + \hat{k}E_z \quad (5)$$

$$\bar{v}_d = \hat{i}v_{dx} + \hat{j}v_{dy} + \hat{k}v_{dz} \quad (6)$$

$$\bar{B} = \hat{i}B_x + \hat{j}B_y + \hat{k}B_z \quad (7)$$

$$\begin{aligned} \bar{v}_d \times \bar{B} &= \begin{vmatrix} \hat{i} & \hat{j} & \hat{k} \\ v_{dx} & v_{dy} & v_{dz} \\ B_x & B_y & B_z \end{vmatrix} \\ &= \begin{vmatrix} \hat{i} & \hat{j} & \hat{k} \\ v_{dx} & 0 & v_{dz} \\ 0 & 0 & B_z \end{vmatrix} = -\hat{j}v_{dx}B_z \end{aligned}$$

$$F_x = m_{n,eff} \frac{d^2x}{dt^2} = qE_x = q \frac{V_{DS}}{L} \quad (8a)$$

$$F_y = m_{n,eff} \frac{d^2y}{dt^2} = q(E_y - v_{dx}B_z) = q \left(E_y - \frac{dx}{dt} B_z \right) \quad (8b)$$

$$F_z = m_{n,eff} \frac{d^2z}{dt^2} = 0 \quad (8c)$$

Equation (8a) can be solved to obtain the instantaneous drift velocity of electrons along the channel (v_{dx}) and also its position (x) in equations (9a) and (9b) respectively under the following assumptions:

$$\text{At } t = 0, x = 0 \text{ and } v_{dx} \Big|_{t=0} = v_{d,sat} = \mu_{n,eff} \frac{V_{DS}}{L} .$$

$$v_{dx} = \frac{dx}{dt} = \frac{qV_{DS}}{m_{n,eff}L} t + v_{d,sat} \quad (9a)$$

$$x = \frac{qV_{DS}}{2m_{n,eff}L} t^2 + v_{d,sat} t \quad (9b)$$

Time required for an electron to travel along the channel from source to drain is called transit time. So, at $t = t_r$, $x = L$ and solving equation (9b) we get equation (10) for transit time.

$$t_r = -\frac{v_{d,sat} m_{n,eff} L}{qV_{DS}} + \frac{m_{n,eff} L}{qV_{DS}} \sqrt{v_{d,sat}^2 + \frac{2qV_{DS}}{m_{n,eff}}} \quad (10)$$

Equation (8b) is solved to get the instantaneous electron deflection/trajectories perpendicular to the channel as in equation (11) under the following assumptions:

$$\text{At } t = 0, y = 0 \text{ and } v_{dy} = \left. \frac{dy}{dt} \right|_{t=0} = 0.$$

$$\Delta y = \frac{q}{m_{n,eff}} \left[E_{y,eff} \frac{t^2}{2} - \left(\frac{qV_{DS}}{m_{n,eff}L} \frac{t^3}{6} + v_{d,sat} \frac{t^2}{2} \right) B_z \right] \quad (11)$$

,where $E_{y,eff}$ is the effective normal electric field, (along the y-direction as given in equations (14)) which is the summation of the effective normal electric field [40] along the y-direction due to the application of gate voltage as given in equation (12) and Hall electric field generated [41] along the y-direction due to the application of magnetic field along the z-direction as given in equation (13).

$$E_{yN} = \frac{C_{ox}}{\epsilon_{Si}} (\eta(V_{GS} - V_{th}) + V_{th} - V_{FB} - 2\psi_{s,inv}) \quad (12)$$

$$E_{yH} = -\frac{1}{qN_{eff}} J_x B_z \quad (13)$$

$$E_{y,eff} = E_{yN} + E_{yH} \quad (14)$$

,where $\psi_{s,inv}$ is the surface potential at inversion condition and V_{th} is the threshold voltage of the pocket implanted n-MOSFET obtained from [42] and [43] respectively; V_{GS} and V_{FB} are the gate and flat band voltages respectively, J_x is the subthreshold drain current along the x-direction obtained from [6], B_z is the magnetic flux density applied along the z-direction.

Drain current sensitivity, S along the positive y-axis is defined in equation (15).

$$S = \left| \frac{\Delta y(B \neq 0) - \Delta y(B = 0)}{B_z \Delta y(B = 0)} \right| \quad (15)$$

,where $\Delta y(B \neq 0)$ and $\Delta y(B = 0)$ are the drain current deflections without and with the presence of magnetic field.

3 Simulation Results

The drain current deflection of MFS-based pocket implanted n-MOSFETs was simulated for different values of device and pocket profile parameters. In Figs. 2-3, direction of magnetization perpendicular to the channel was changed to observe the change of direction of drain current deflection. It is observed that as the magnetization is increased the magnitude of drain current deflection is increased. Besides, if gate voltage is increased the magnitude of drain current deflection is also increased. Because, when gate voltage is increased, the effective normal electric field is increased. This field is additive/ subtractive with the Hall electric field produced due to the Lorentz force generation when the magnetic field is applied perpendicular to the direction of drain current flow.

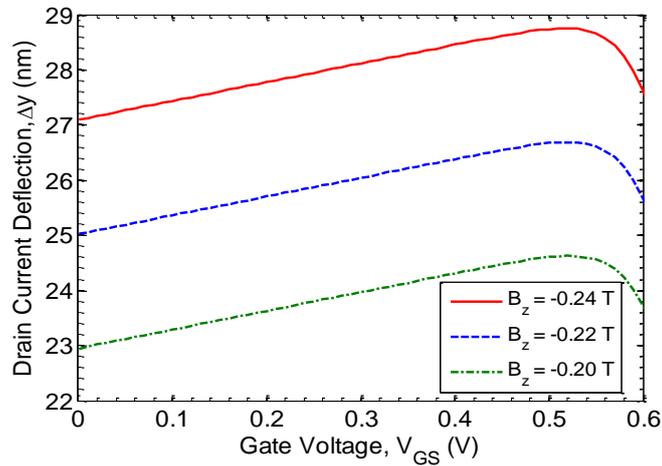


Fig. 2. Drain current deflection in the positive y-direction with gate-to-source voltage variation for different magnetic flux density in the negative y-direction.

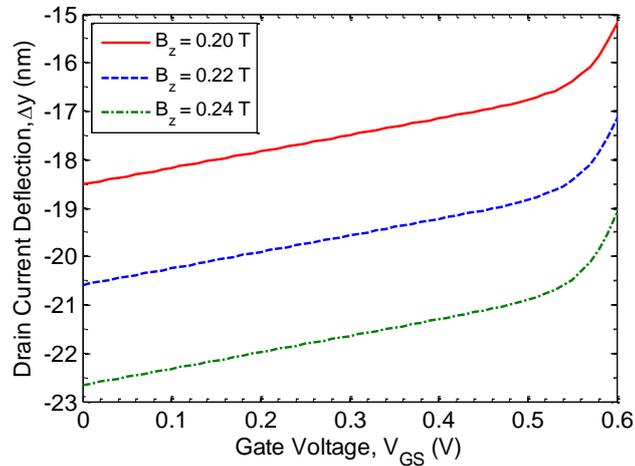


Fig. 3. Drain current deflection in the negative y-direction with gate-to-source voltage variation for different magnetic flux density in the positive y-direction.

In Fig. 4, if oxide thickness is increased then the magnitude of drain current deflection is decreased for a particular gate voltage due to the decrement of effective normal electric field. That is, if nano scale MOSFET is to be used then oxide thickness needs to be decreased then the amount of drain current deflection will decrease. To compensate this effect pocket doping can be introduced so that the deflection can be increased.

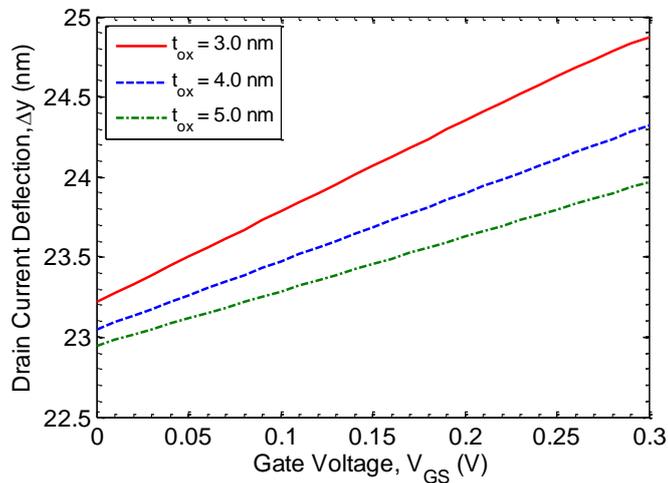


Fig. 4. Drain current deflection in the negative y-direction with gate-to-source voltage variation for different gate oxide thicknesses with $B = -200$ mT.

In Figs. 5-6, if pocket length or peak pocket doping concentration is increased then the magnitude of drain current deflection is also increased for a particular gate voltage due to the increment of effective normal electric field. That is, the introductions of pocket doping near the source or drain edges can increase the amount of drain current deflection for the nano scale n-MOSFET.

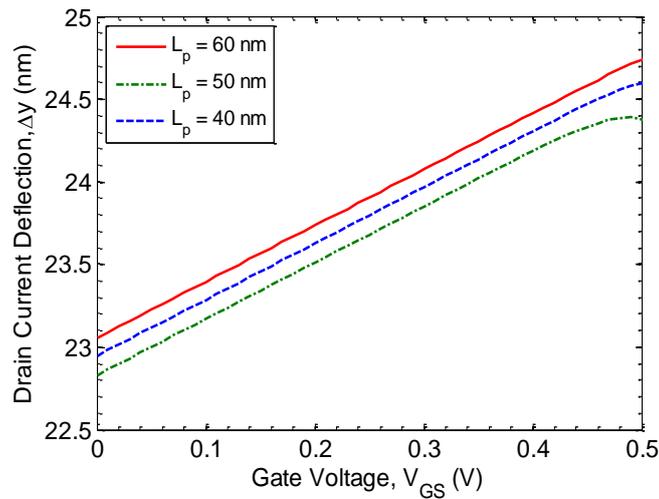


Fig. 5. Drain current deflection in the positive y-direction with gate-to-source voltage variation for different pocket lengths with $B = -200$ mT.

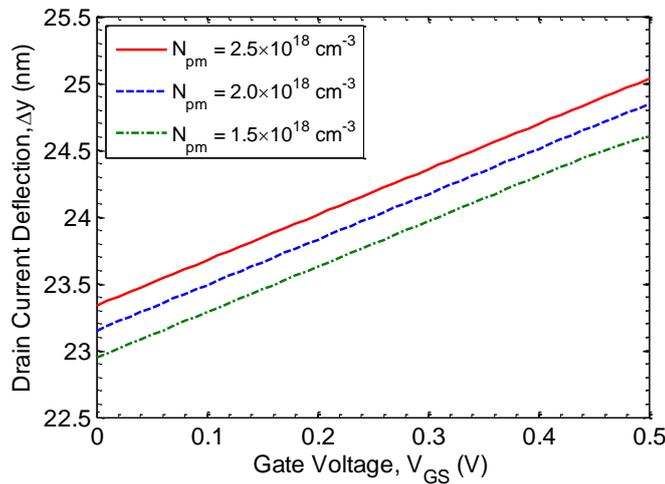


Fig. 6. Drain current deflection in the positive y-direction with gate-to-source voltage variation for different peak pocket doping concentration with $B = -200$ mT.

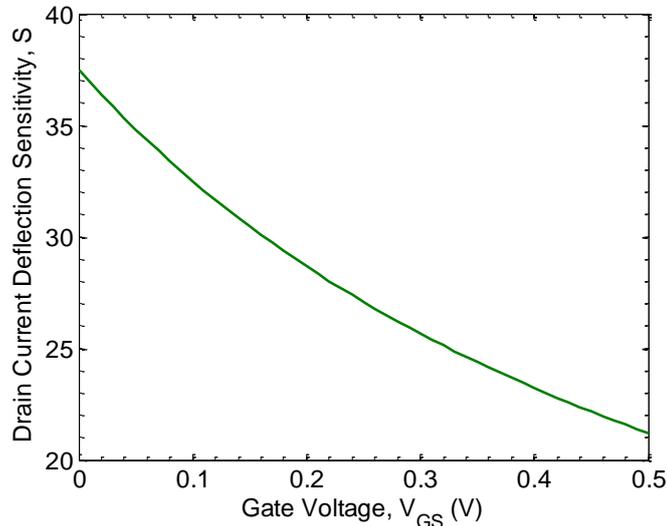


Fig. 7. Drain current deflection sensitivity vs. gate-to-source voltage with $B = -200$ mT for channel length of 100 nm.

In Fig. 7, drain current deflection sensitivity, S along the positive y -direction with gate-to-source voltage variation is shown with magnetic flux density of -200 mT perpendicular to the direction of drain current. The nature of this curve is very similar to the result of drain current sensitivity, S of Fig. 5 in [44].

4 Conclusions

In this paper, a semi-analytical subthreshold drain current deflection model of MFS-based pocket implanted n-MOSFET in nano scale regime has been developed. Subthreshold drain current model based on the conventional drift-diffusion equation, surface potential as well as the threshold voltage models for the pocket implanted n-MOSFETs incorporating the effects of substrate and drain bias dependencies are used. The model is developed assuming two linear symmetric pocket doping profiles along the channel at the surface of the device from the source and drain edges. The effects of changing the device and pocket profiles parameters as well as magnetic flux density's magnitude and direction on the subthreshold drain current deflection have been studied using the proposed model. The simulated results show that the proposed model predicts the subthreshold current deflection for the channel lengths in the nano scale regime. Subthreshold drain current deflection sensitivity calculation shows similar trend found in the literature. Hence this model efficiently evaluates the subthreshold drain current deflection of scaled pocket implanted n-MOSFETs having channel lengths in the nano scale regime.

References

1. W. M. Penney, L. Lau: MOS Integrated Circuits, Microelectronics Series, Van Nostrand Rein. Comp., New York, USA, ch. 2, § 3.4, §4.6; ch. 3, §4.1 (1972).
2. R. S. C. Cobbold: Theory and Application of Field-Effect Transistors, Wiley-Interscience a Division of John and Sons, New York, USA, ch. 7, §1; §2 (1970).
3. J. T. Wallmark, H. Johnson: Field-Effect Transistors, Prentice-Hall, Englewood Cliffs, New Jersey, USA, ch. 5, §2(6).
4. S. M. Sze: Physics of Semiconductor Devices, 2nd edition, John Wiley and Sons Inc., NY, USA, ch. 8, (1981); and S. M. Sze: Semiconductor Devices, John Wiley and Sons Inc., NY, USA, (2001).
5. H. Baltes, R. Popovic: Integrated Semiconductor Magnetic Field Sensor, Proc. of IEEE IEDM Technical Digest, 74, p. 1107 (1986).
6. M. H. Bhuyan: Analytical Modeling of the Pocket Implanted Nano Scale n-MOSFET, PhD Thesis, Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, July, (2011).
7. A. Chatterjee, J. Liu, P. K. Mozumder, M. Rodder and I. C. Chen: Pass transistor designs using pocket implant to improve manufacturability for 256-Mbit DRAM and beyond, in Proceedings of IEEE IEDM Technical Digest, p. 87 (1994).
8. N. R. Santiago: Characterization, Modeling and Simulation of Decananometer SOI MOSFETs, PhD Thesis, Department of Electronics Technology, University of Grenada, Spain, (2007).
9. M. Saxena, S. Haldar, M. Gupta, et al: Design considerations for novel device architecture: hetero-material double-gate (HEM-DG) MOSFET with sub-100 nm gate length, Solid-State Electronics, vol. 48, no. 7, pp. 1167-1174, (2004).
10. M. J. Kumar and A. Chaudhry: Two-dimensional analytical modeling of fully depleted SHDMG SOI MOSFET and evidence for diminished SCEs, IEEE Transactions on Electron Devices, vol. 51, no. 4, pp. 569-674, (2004).
11. K. Likharev: Single-electron devices and their applications, Proc. of IEEE IEDM Technical Digest, vol. 87, pp. 606-632, April (1999).
12. S. Ben Dhia, M. Ramdani, and E. Sicard: Electromagnetic Compatibility of Integrated Circuits: Techniques for Low Emission and Susceptibility, 1st ed. Springer Science, p. 1 (2006).
13. S. Aoyama, S. Kawahito, T. Yasiu, and M. Yamaguchi: IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging, p. 103 (2005).
14. B. Deutschmann and R. Jungreithmair: IEEE International Symposium on Electromagnetic Compatibility, p. 1125 (2003).
15. N. Ando, N. Masuda, N. Tarnaki, T. Kuriyama, S. Saito, K. Kato, K. Ohashi, M. Saito and M. Yarnaguchi: Miniaturized thin-film magnetic field probe with high spatial resolution for LSI chip measurement, International Symposium on Electromagnetic Compatibility (EMC), vol. 2, pp. 357-362 (2004).

16. E. Suzuki, S. Arakawa, M. Takahashi, H. Ota, K. Ichi Arai, R. Sato: Visualization of Poynting Vectors by Using Electro-Optic Probes for Electromagnetic Fields, *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 5, p. 1014-1022 (2008).
17. K. Nakano, T. Takahashi, S. Kawahito: A CMOS Rotary Encoder Using Magnetic Sensor Arrays, *IEEE Sensors Journal*, vol. 5, no. 5 pp. 889-894, May (2005).
18. A. Ali, D. K. Potter: A new contactless trackball design using Hall effect sensors, *Sensors and Actuators, A* 147, pp.110-114, April (2008).
19. W. Hernandez: Improving the Response of a Rollover Sensor Placed in a Car under Performance Tests by Using a RLS Lattice Algorithm, *Sensors Journal, Molecular Diversity Preservation, International*, vol. 5, pp.613-632, (2005).
20. F. Ayazi, K. Najafi: Design and Fabrication of A High-Performance Polysilicon Vibrating Ring Gyroscope, *IEEE/ASME International Workshop on Micro Electro Mechanical Systems*, Heidelberg, Germany, January 25-29, (1998).
21. S. D. Senturia: Perspectives on MEMS, Past and Future: The Tortuous Pathway From Bright Ideas to Real Products, *IEEE, International Conference on Solid State Sensors, Actuators and Microsystems*, Boston, June 8-12, (2003).
22. B. Ziaie, T.W. Wu, N. Kocaman, K. Najafi, and D.J. Anderson: An Implantable Pressure Sensor Cuff for Tonometric Blood Pressure Measurement, *Technical Digest, Solid-State Sensor and Actuator Workshop*, June, (1998).
23. D. Mavrudieva, J.-Y. Voyant, A. Kedous-Lebouc, J.-P. Yonnet: Magnetic structures for contactless temperature sensor, *Sensors and Actuators, A* 142, pp. 464-467, (2008).
24. Y. JaeJun, S. KyoungBok and J. JungAh: Intelligent Non-signalized Intersections Based on Magnetic Sensor Networks, *IEEE Intelligent Sensors, Conference on Sensor Networks and Information*, pp. 275-280 (2007).
25. C. Schott, R. Racz, A. Manco, and N. Simonne: CMOS Single-Chip Electronic Compass with Microcontroller, *IEEE Journal of Solid-state Circuits*, vol. 42, no. 12, pp. 2923-2933, (2007).
26. R. Rodriguez-Torres, R. Klima, and S. Selberherr: Three-Dimensional Analysis of a MAGFET at 300 K and 77 K, *ESSDERC*, pp. 151-154 (2002).
27. R. Rodriguez-Torres, E. A. Gutierrez-Dominguez, R. Klima and S. Selberherr: Analysis of Split-Drain MAGFETs, *IEEE Transactions on Electron Devices*, vol. 51, no. 12, pp. 2237-2245, (2004).
28. A. Nathan, W. Allegretto, H. P. Baltes and Y. Sugiyama: Carrier Transport in Semiconductor Detectors of Magnetic Domains, *IEEE Transactions on Electron Devices*, vol. 34, no. 10, pp. 2077-2085, (1987).
29. P. J. Garcia-Ramirez, J. Martinez-Castillo and A. L. Herrera-May: A Semi-Analytical Model of a Split-Drain MAGFET Sensitivity at Room Temperature, *Euroensors Conference*, Barcelona, Spain, 11-14 September (2005).
30. P. J. G. Ramirez and F. S.I Ibarra: Performance of a MFS-Based MOSFET for Low Temperature Applications, *Journal of Applied Research and Technology*, vol. 1, pp. 37-43, April (2005).

31. P. Garcia, R. Murphy and E. Gutierrez: Analysis of a silicon magnetic sensor at 77K, Memoria del Workshop International IBERCHIP, pp. 1-5, April (2002).
32. T. Pesic-Brdanin, N. Jankovic and D. Pantic: SPICE MAGFET Model and its Application for Simulation of Magnetically Controlled Oscillator, IEEE International Conference on Microelectronics, NIS, Serbia, 11-14 May (2008).
33. Y. S. Pang and J. R. Brews: Models for subthreshold and above subthreshold currents in 0.1 μm pocket n-MOSFETs for low voltage applications, IEEE Transactions on Electron Devices, vol. 49, pp. 832-839, May (2002).
34. C. S. Ho, J. J. Liou, K.-Y. Huang and C.-C. Cheng: An analytical subthreshold current model for pocket implanted NMOSFETs, IEEE Transactions on Electron Devices, vol. 50, pp. 1475-1479, June (2003).
35. K. M. Jackson: Laterally non-uniform doping profiles in MOSFETs: modeling and analysis, M.Sc. Engg. Thesis, Dept of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, USA, ch. 2, August (1996).
36. X. Zhou, K. Y. Lim and D. Lim: Physics-Based threshold voltage modeling with Reverse Short Channel Effect, Journal of Modeling and Simulation of Microsystems, vol. 2, no. 1, pp. 51-56, (1999).
37. X. Zhou, K. Y. Lim and D. Lim: A general approach to compact threshold voltage formulation based on 2-D numerical simulation and experimental correlation for deep-submicron ULSI technology development, IEEE Trans. on Electron Devices, vol. 47, no. 1, pp. 214-221, January (2000).
38. M. H. Bhuyan and Q. D. M. Khosru: Linear Pocket Profile Based Threshold Voltage Model for Sub-100 nm n-MOSFET Incorporating Substrate and Drain Bias Effects, Proceedings of the 5th IEEE International Conference on Electrical and Computer Engineering, Dhaka, Bangladesh, December 20-22, pp. 447-451, (2008).
39. A. Nussbaum, R. Sinha and D. Dokos: The theory of the long-channel MOSFET, Solid State Electronics, vol. 27, no. 1, pp. 97-106, January (1984).
40. M. H. Bhuyan and Q. D. M. Khosru: Inversion Layer Effective Mobility Model for Pocket Implanted Nano Scale n-MOSFET, International Journal of Electrical and Electronics Engineering, vol. 5, no. 1, pp. 50-57, Winter (2011).
41. E. Hall: On a New Action of Magnet on Electric Currents, American Journal of Mathematics, vol. 2, p. 287, (1879).
42. M. H. Bhuyan and Q. D. M. Khosru: An Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET, Proceedings of the International Conference on Electrical and Computer Engineering, Dhaka, 20-22 December, pp 442-446, (2008).
43. M. H. Bhuyan and Q. D. M. Khosru: Linear Pocket Profile Based Threshold Voltage Model for Sub-100 nm n-MOSFET, International Journal of Electrical and Computer Engineering, vol. 5, no. 5, pp. 310-315, May (2010).
44. B. O. Onodipe and M. G. Guvench: Transverse Magnetic Field Effects on GaAs MESFETS: Analytical Model and Experiments, 8th IEEE University/Government/Industry Symposium, pp. 215-218, (1989).