Minimizing Clock Power Wastage By Using Conditional Pulse Enhancement Scheme

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Abstract: In this paper, a low-power pulse-triggered flip-flop (FF) designed and a simple two-transistor AND gate is designed to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 50-nm technology reveal that the proposed design features the best power-delay-product performance in several FF designs under comparison. Its maximum power saving against rival designs is up to 18.2% and the average leakage power consumption is also reduced by a factor of 1.52.

Keywords: Flip-flop, low power, pulse-triggered, pulse enhancement.

1. Introduction

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a days often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–40% of the total system power [1].Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network [4].Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the Pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated.
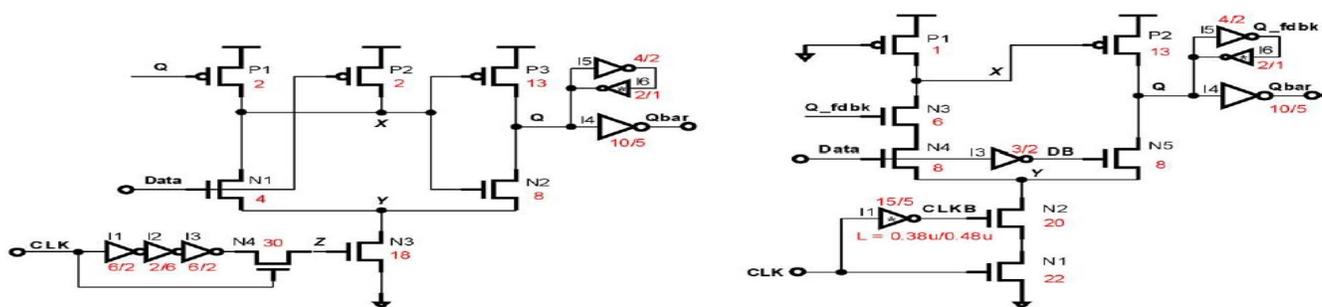
Fig.1. Conventional pulse-triggered FF designs
(a) MHLLF (b) SCCER

In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives rise to competitive power and power–delay–product performances against other P-FF designs.

2. Implicit-Type P-Ff Design With Pulse Control Scheme

2.1   Conventional Implicit-Type P-Ff Designs

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters. Two practical problems exist in this design. First, during the rising edge, PMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

Fig. 1(b) shows an improved P-FF design, named MHLLF, by employing a static latch structure presented. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistorP1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero. This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1"transitions because node x is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact"1". Fig. 1(a)) is replaced by a weak pull up transistor P1 in conjunction. The discharge path contains MOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistorP1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

2.2   Proposed P-FF Design

The proposed design, as shown in Fig. 2, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of NMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 2, the upper part latch design is similar to the one employed in SCCER design .As opposed to the transistor stacking design in Fig. 1(a) transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two NMOS transistors

(N2and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.
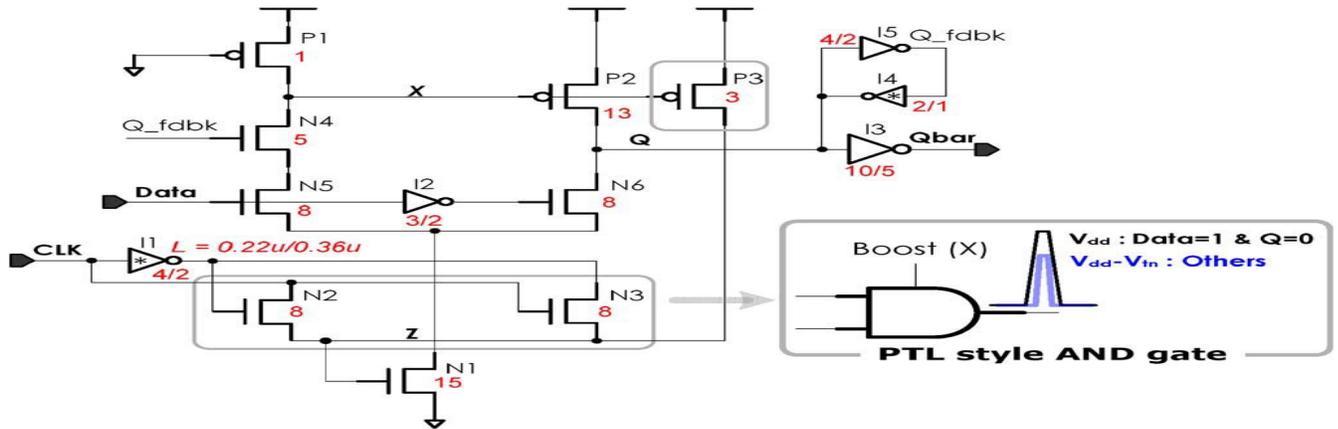
Fig 2. Schematic Diagram of the proposed P-FF design with pulse enhancement scheme.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time. It steps in when node X is discharged to VTP below the VDD. This provides additional boost to node X (from VDD-VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor N1.After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1.

3. Simulation Results

To demonstrate the superiority of the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the two P-FF designs shown in Fig. 1 (MHLLF, SCCER), The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0 V.

P-FF	MHLFF	SCCER	PROPOSED
Numberof transitors/Layout Area(μm^2)	19/93.02	17/80.07	19/79.2
Setup time(ps)	8.3	-58.1	-39.7
Hold time(ps)	82.2	59.3	85.1
Min data to Q Delay(ps)	177.1	112.9	107.2
Clock tree power μW	7.82	12.58	8.03
Averagepower (100%Activity)μW	35.96	36.27	31.11
Averagepower (50%Activity)μW	27.61	28.46	22.65
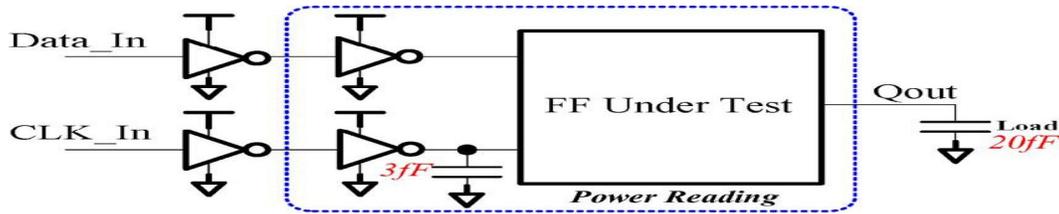
Fig. 3. Simulation setup model.

In general, the MHLLF design has the worst PDP_{DQ} performance due to the drawback of its latch structure. Fig. 6(a) shows the best PDP_{DQ} performance of each design under different data switching activities. The proposed design takes the lead in all types of data switching activity. The SCCER and the MHLFF designs almost tie in the second place. Fig. 6(b) shows the PDP_{DQ} performance of these designs at different process corners under the condition of 50% data switching activity. The performance edge of the proposed design is maintained as well. Notably, the MHLLF design has the worst PDP_{DQ} performance especially at the SS process corner due to a large D-to-Q delay and the poor driving capability of its pulse generation circuit. Table I also summarizes some important performance indexes of these P-FF designs. These include transistor count, layout area, setup time, hold time, min D-to-Q delay, optimal PDP, and the clock tree power.
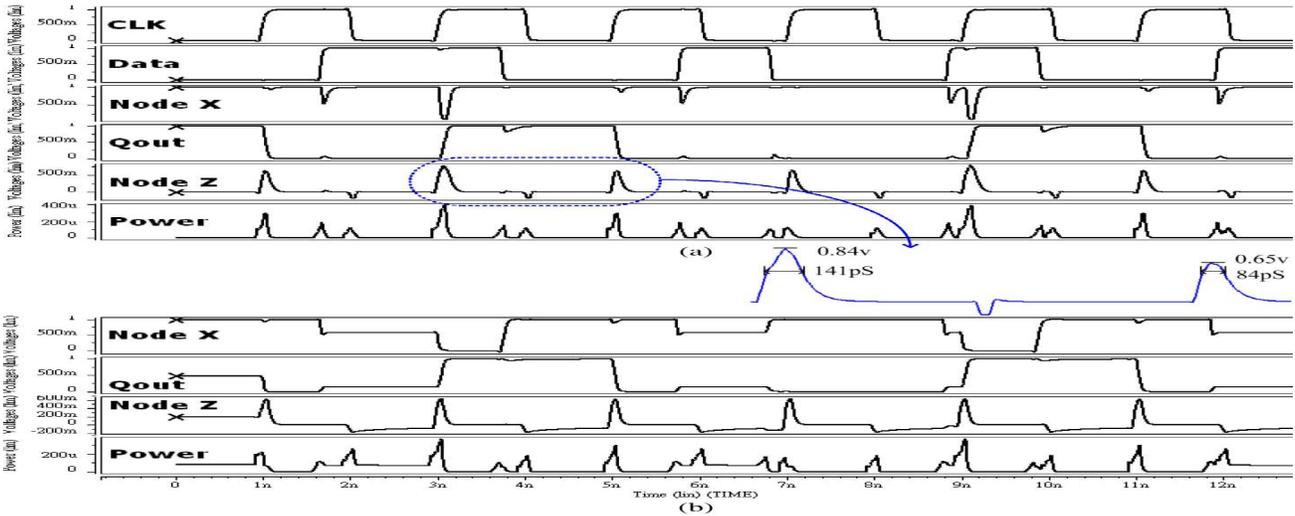
Fig. 4. Simulation waveforms of (a) proposed and (b) MHLLF designs.
Feature Comparison Of Various P-Ff Designs

Although the transistor count of the proposed design is not the lowest one, its actual layout area is the smaller than all but the TGFF design. The MHLLF design exhibits the largest layout area because of an oversized pulse generation circuit. Following the measurement methods in [6], curves of D-to-Q delay versus setup time and C-to-Q delay versus hold time are simulated first. Setup time is defined as the point in the curve where D-to-Q delay is the minimum. Hold time is measured at the point where the slope of the curve equals -1.

The proposed design features the shortest minimum D-to-Q delay. Its hold time is longer than other designs because the transistor (P3) for the pulse enhancement requires a prolonged availability of data input. The power drawn from the clock tree is calculated to evaluate the impact of FF loading on the clock jitter. Although the proposed FF design requires clock signal connected to the drain of transistor N2, the drawn current is not significant. Due to complementary switching behavior ofN2 and N3, there exists no signal path from the entry of the clock signal to either V_{DD} or GND.
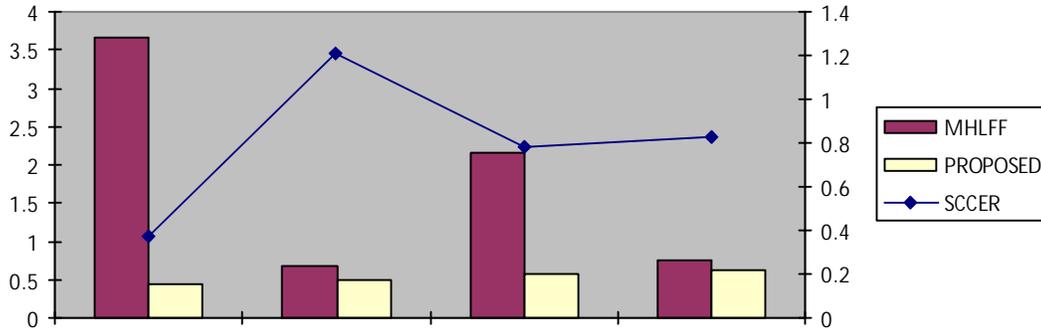
Fig. 5. Power–delay-product performances under (a) different data switching activities and (b) different processor corners at 50% data switching activity. (c) proposed flip in accordance with power dissipation.

3.1 Leakage Power Comparison In Standby Mode (M W)

FF/design/(CLK,Data)	(0,0)	(0,1)	(1,0)	(1,1)
MHLFF	3.656	0.666	2.161	0.763
SCCER	0.369	1.208	0.779	0.823
PROPOSED	0.444	0.481	0.582	0.624

Significantly better than other designs. The simulation results show that the clock tree power of the proposed design is close to those of the two leading designs (MHLFF and SCCER) and out performs of MHLLF, SCCER where clock signals connected to gates of the transistors only. The setup time is measured as the point where the minimum PDP value occurs. The setup times of these designs vary from -67 to +47 ps. Note that although the optimal setup time of the proposed design is -53.9 ps, its PDP value is lowest in all designs for any setup time greater than-60 ps. The D-to-Q delay and the hold time are calculated subject to the optimal setup time. The D-to-Q delay of the proposed design is second to the SCCER design only and out performs the conventional TGFF design by a margin of 44.7%. The hold time requirement seems to be slightly larger due to a negative setup time. This number reduces as the setup time moves toward a positive value. Table II gives the leakage power consumption comparison of these FF designs in a standby mode (clock signal is gated). For a fair comparison, we assume the output Q as "0" when input data is "1" to exclude the extra power consumption coming from the discharging of the internal node X. For different clock and input data combinations, the proposed design enjoys the minimum leakage power consumption, which is mainly attributed to the reduction in the transistor sizes along the discharging path.

3.2 Pulse Generation Against Process Variation ($P_{S/V}$)

Corner case	SS	SF	TT	FS	FF
Data=0	180.1/0.45	92.9/0.61	84.7/0.65	83.1/0.063	50.0/0.77
Data=1	375/.51	167.5/0.86	141.3/0.84	145.4/0.87	87.7/1.04

The SAFF design experiences the worst leakage power consumption when clock equals "0" because its two precharge PMOS transistors are always turned on. Compared to the conventional TGFF design, the average leakage power is reduced by a factor of 3.52. Finally, to show the robustness of the proposed design against the process variations, Table III compiles the changes in the width and the height of the generated discharge pulses under different process corners. Although significant fluctuations in pulse width and height are observed, the unique conditional pulse-enhancement scheme works well in all cases.

Conclusion

In this paper, we design a novel low-power pulse-triggered FF design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, D-to-Q delay, and PDP. Coupled with these design merits is a longer hold-time requirement inherent in pulse-triggered FF designs. However, hold-time violations are much easier to fix in circuit design compared with the failures in speed or power.

Acknowledgement

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