International Journal of Computer Engineering Science (IJCES)
Volume 3 Issue 5 (May 2013) ISSN : 2250:3439
https://sites.google.com/site/ijcesjournal http://www.ijces.com/

SSBD: Single Side Buffered Deflection Router for On-Chip Networks

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***Abstract*:** As technology scaling drives the no.of processors upward, current on-chip routers consume substantial portions of chip area, performance, cost & power budgets. Recent work proposes to apply well-known routing technique, which eliminate buffers & hence buffers power (static & dynamic) at the cost of some misrouting or deflection called bufferless deflection routing. While bufferless NoC design has shown promising area and power reductions and offers similar performance to conventional buffered for many workloads. Such design provides lower throughput, unnecessary networkhops and wasting power at high network loads.

To address this issue we propose an innovative NoC router design called Single Side Buffered Defection (SSBD)router. Compared to previous bufferless deflection router SSBD contributes (i) a router microarchitecture with a double-width ejection path and enhanced arbitration with in-router prioritization. (ii)small side buffers to hold some traffic that would have otherwise been deflected.

Keywords: Networks–on-Chip, Deflection Routing, LiveLock, DeadLock,

1. Introduction

As the number of core counts in systems-on-chip(SoCs)[5] increases,bus-based interconnection architectures may prevent these systems to meet the performance required by many applications. A solution for such a communication bottleneck is the use of an embedded switching network called Network-on-Chip(NoC),to interconnect the core's in SoCs. Unfortunately, packet-switched NoCs are projected to consume significant power [17]

Mechanisms have been proposed to make conventional Virtual channeled input buffered NoC routers more energy efficient[18][19].Bufferless deflection routers[6],[10] removes router input buffers completely to reduce router power. Removing buffers yields more energy efficient NoC designs: e.g.,CHIPPER[6] & BLESS[10]. Unfortunately at high network traffic, deflection routing reduces performance significantly because of higher deflection rate.We propose Single Side-buffered deflection router (SSBD) as a new NoC router design that combines both bufferless and buffered mechanisms. When two flits request the same output port, the router deflects one of them to another output port.However,the router can choose to buffer one deflected flit per cycle rather than deflecting it.

As we show in our evaluations, SSBD shows better performance relative to the buffeless router and approaching conventional buffered router performance.

2. Background

In this section, we give brief scope on NoC-based cache-coherent CMPs, and on bufferless deflection routing, which we build upon. We assume the reader is familiar with the basic operation of conventional input-buffered routers; Dally and Towles [9] provide a good reference on these routers.

2.1 NoCs in cache-coherent CMPs:

NoC form the backbone of memory systems in most recently-proposed and prototyped large-scale CMPs (chip multiprocessors) [12], [7], [16]. Each core, shared cache or memory controller is part of one "node" in the network and network nodes exchange packets that request and respond with data in order to fulfill memory accesses.

2.2 Bufferless Deflection Routers:

Bufferless deflection routing was first proposed by Baran [1]. It has found tremendous interest in NoC design because on-chip links or channels are relatively cheap compared to buffers which consume significant power [10], [8], [4], [2], [3]. For deliver guarantee Priority schemes such as age based priorities were used for an early implementation of bufferless deflection routing BLESS [10], and CHIPPER [6] CHIPPER is a baseline in our evaluations.

3. Motivation

For low-to-medium traffic, a bufferless router[6], [10] has performance close to a conventional buffered router because deflection rate is low. However as the injection rate increases i.e. load increases, the deflection rate is going to be increased in a bufferless deflection network. The higher deflection rate cause each flit to take a longer path to reach its destination and this increased latency reduces the system performance motivated largely by the observation that many NoCs in CMPs are over provisioned for the common-case network load. In this case, a bufferless network can attain nearly the same application performance while consuming less power, which yields higher energy efficiency.But,if we use a conventional buffered router to obtain higher performance at high load, then energy efficiency is poor, because input buffers stores all incoming flits.This motivates us to introduce single side buffered deflection router which will store a portion of deflected flits approaching the performance of buffered.

4.SSBD:Single Side-Buffered Deflection Router

The SSBD router is a new innovative NoC router design that combines bufferless deflection routing with a small single buffer, called “side buffer.” We will explain the operation of the SSBD router in stages First 4.1 explain the deflection routing the 4.2 explains buffering of deflected flits and 4.3 explains injection and ejection of the flits into the router and out of the router respectively. Finally 4.4 describes the delivery guarantee issues.

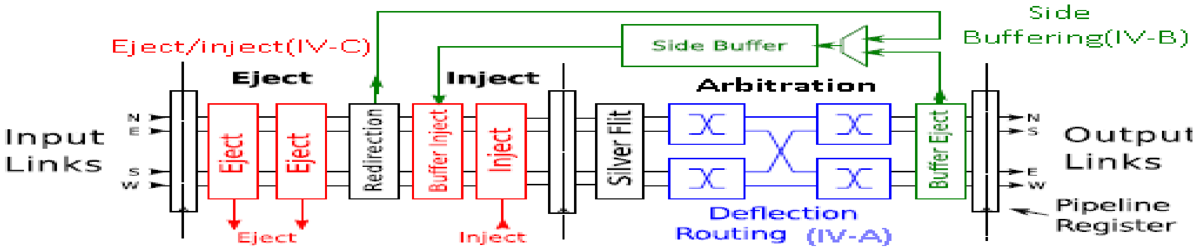

Fig 1 :SSBD router pipeline

Algoritm1: Arbitration in the permute stage(based on Golden Packet[6] with new condition

```
At each cycle in permute stage:
Given: two flits,each of which is golden, silver or ordinary
if GoldenTie then
   Resolve ties between two golden flits by sequence number
   elseif Golden Dominance then
         Golden flit wins over any silver or ordinary flits
   elseif silver Dominance then
        Silver flits win over ordinary flits
   else resolve ties between ordinary flits randomly
endif
```

4.1 Bufferless Deflection Routing

The SSBD router pipeline is shown in Fig. 1. Flits from the neighbor router and local node travel through pipeline form input links to output links.SSBD uses the deflection router organization proposed in CHIPPER[6]. The permutation network in the arbitration stage consists of two stages of two input arbiters.

Each two input arbiter block determines which flit has highest priority among the two flits and sends the highest priority flit to the preferred output direction; The other flit at the arbiter block, send to another output port if any. To ensure Livelock freedom of flits we modified Golden priority scheme[6] to ensure delivery guarantee and forward progress. The modified prioritization rules are described in Algorithm1**.**

4.2 Single Side Buffer to Reduce Deflections

The performance issue addressed by SSBD is increased deflection rate at high load. To address this unlike, a bufferless deflection router,our SSBD router uses a small single side buffer which can buffer one deflected flit per cycle. From the Side Buffer flits are reinjeted into the network whenever a free slot is available in the input links. Algorithm2 describe the side-buffer behavior in the arbitration stage .

Algorithm2 Insertion into the Side-Buffer

```
At each cycle, in permute stage:
Perform  bufferless deflection routing
for each deflected flit fi at output of permute stage do
    if not currently purging buffer and fi is not golden and
       fi is not addressed to current node then mark flit as $f_{buffer}$
    end if
end for
if at least one flit is $f_{buffer}$ then
   randomly pick one flit $f_{buffer}$
   remove $f_{buffer}$  from router and place into side-buffer
end if
```

4.3 Injection and Ejection

So far, we have considered the flow of flits from router input ports to router output ports. When a set of flits arrive at input links,these flits first pass through the Eject/Inject stage. The ejection logic examines destination of each flit and if a flit is addressed to the local node, it is removed from the router and sent to the local node. However if more than one flit is belongs to locally destined node then according to priority scheme used by routing arbitrations one flit is deflected. Because bufferless deflection router can eject only one flit per cycle.

Algoritm3: Ejection of flits from the Ejection port

```
At each cycle in ejection stage:
for each injected flit $f_{inj}$ do
    if either one or two $f_{inj}$ addressed to current node then mark $f_{inj}$ as eject-eligible
       Pick highest-priority locally destined flit $f_{eject}$, remove $f_{eject}$ from  router pipeline and eject
       it to the local node
    endif
endfor
```

However, ejecting a single flit per cycle can produce a bottleneck and cause unnecessary deflections for flits that could not be ejected. To address this issue one more ejection block is added . This will eject two flits/node/cycle. Algorithm3 and Algorithm4 describes the ejection of flits to the local node and ejection of buffered flits from the Side Buffer in to the buffer.

Algorithm 4 Ejection of buffered flits from the Side Buffer:

```
At each cycle, in eject/inject stage:
if currently purging buffer then
   if side-buffer is not empty then
      select one flit after eject (before redirection) stage,  send to side-buffer tail take a flit from side-buffer head, re-inject into router
   else
      complete side-buffer purging
   end if
else
   if  side-buffer is not empty and at least one free slot is available then take a flit from side-buffer head and place in router
   end if
endif
```

4.4 Ensuring Side Buffered Flits Make Forward Progress

If a deflected flit enters the side-buffer,it must be re-injected later. For this buffer inject block has been provided in the router. But there is a possibility that a free slot will not appear for a long time so, that flits well not reinjected for a long time i.e., no forward progress of flits. To avoid this buffer starvation problem, we implement buffer redirection. If a free slot is not available for more than some threshold $T_{hreshold}$ then one flit from the router input is randomly picked and is forced in the side buffer simultaneously, the flit at the head of the side buffer is allowed to enter to the free slot. Algorithm5 describes buffer purging to prevent buffer starvation.

Algorithm 5 Buffer Purging to Prevent Buffer Starvation

```
Initially:
$B_{blocked} \leftarrow 0$
At each cycle:
if the side-buffer is not empty and re-injection is blocked then
   if $B_{blocked} < B_{threshold}$ then
      $B_{blocked} \leftarrow B_{blocked} + 1$
   else
      $B_{blocked} \leftarrow 0$
      enter buffer-purge mode for one cycle
   end if
else
      $B_{blocked} \leftarrow 0$
end if
```

4.5 Livelock and Deadlock-free Operation

SSBD provides livelock-free delivery guarantee of flits using Modified Golden Packet scheme and buffer redirection. SSBD achieves deadlock-free operation by using Retransmit-Once [6], which ensures that every node always consumes flits delivered to it by dropping flits when no reassembly/request buffer is available.

5. Evaluation

In this section, we evaluate SSBD against a bufferless deflection router [6] and an Virtual Channeled input-buffered router with buffer bypassing [15], [9] and demonstrate that by using a combination of deflection routing and buffering, SSBD achieves performance approaching the conventional input-buffered router .

5.1 Network Level Performance

The Network performance of SSBD was studied by applying three traffic patterns:Uniform random traffic,bit-complement & transpose.Fig. 2 shows Latency as performance metric with different injection rates for the CHIPPER,SSBD,(4,1) & (8,8) conventional input buffered router.

In uniform random traffic SSBD performs better than bufferless router but, almost identically to the base-line buffered router,inspite of having much less buffer space. But the non-uniform patterns particularly bit-complement presents a more challenging workload for SSBD.The buffers in the buffered router help to handle the traffic with less contention than CHIPPER & SSBD.

In addition in the case of transpose traffic pattern the buffered router saturates earlier than the CHIPPER & SSBD because the pattern forces all traffic across the mesh's diagonal

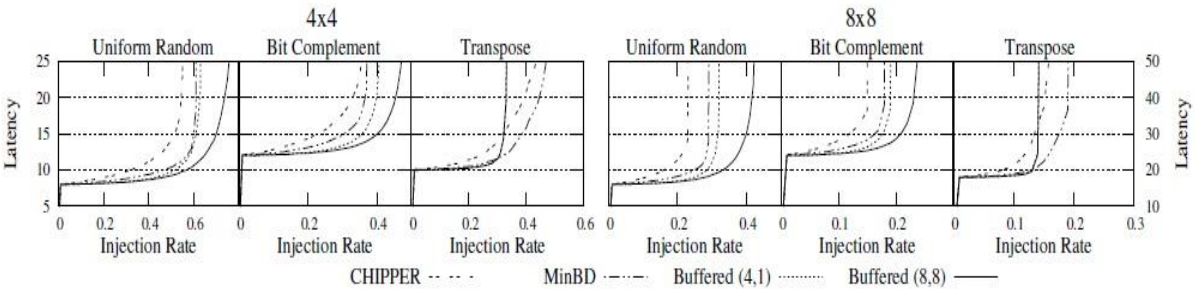

Fig.2. Network-level Performance evaluations for SSBD, CHIPPER and input-buffered routers((4,1) & (8,8)) by applying different traffic patterns in 4x4 and 8x8 mesh NoC topologies.

5.2 Hardware Cost: Router Area

Next we study the impact of mechanism on router area. Table shows router area normalized to the CHIPPER.SSBD adds only 3% area overhead is due to adding side-buffer as well as control logic for dual width ejection and deflection arbitration mechanisms. In both CHIPPER and SSBD the area overhead is less because of area-efficient datapath. From the table the buffered(8,8) router has area of 2.06 normalized to the CHIPPER. Even the smallest input buffered(4,1) has area 60% greater than the CHIPPER & 55% greater than SSBD because of simplified datapath in SSBD.Overall, SSBD reduces area relative to conventional input buffered router

Router Design	CHIPPER	SSBD	Buffered (8,8)	Buffered(4,1)
Normalized Area	1.00	1.03	2.06	1.60

Table: *Normalized Router Area comparision for CHIPPER and Buffered router designs, compared to SSBD*

6. Related Work

To our knowledge, SSBD is the first NoC router design that combines deflection routing with a small side buffer that reduces deflection rate.

6.1.Improving high-load performance in bufferless networks: By reducing network load, source throttling reduces deflection rate and improves overall performance and fairness. These congestion control techniques and others (e.g., [13]) are orthogonal to SSBD, and could improve SSBD's performance further.

6.2.Reducing cost of buffered routers: The Combination both SSBD and empty-buffer-bypassed buffered routers avoid buffering significant traffic, SSBD further reduces router power by using much smaller buffers.

7. Conclusion

In this paper we, present SSBD (Lightly-Buffered Deflection Router) introduces Side buffer to hold only flits that would have been deflected: Dual-width ejection to address ejection bottleneck and two-level prioritization to avoid unnecessary deflections. We conclude that SSBD yields reduced area (36%) relative to buffered routers and yields improved performance (8.1% at high load) relative to bufferless routers. So SSBD achieves competitive performance relative to conventional buffered router

Acknowledgments. I V.Sankaraiah would like to thank Mr. V.Murali Praveen, Asst.Professor of ECE Department, who had been guiding throughout the project and supporting me in giving technical ideas about the paper and motivating me to complete the work effectively and successfully.

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