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A New Current-Mode Sigma Delta Modulator

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Abstract. In this paper, a alternative structure method for continuous time sigma delta modulator is presented. In this modulator for implementation of integrators in loop filter second generation current conveyors are employed. The modulator is designed in CMOS technology and features low power consumption (<2.8mW), low supply voltage (±1.65), wide dynamic range (>65db), and with 180khZ bandwidth. Simulation results confirm that this design is suitable for data converters.

Keywords: Current Conveyor, continuous, sigma delta, MOS.

1 Introduction

In recent years, continuous time (CT) sigma delta modulators have attracted increasingly due to low power consumption, low supply voltage, high sampling frequency and high bandwidth in comparison with similar discrete time sigma delta modulators [1-3]. Moreover, because of placing sampler inside loop filter, charge injection effect and nonlinear sampling switched on resistances are significantly suppressed. In addition, the continuous time loop filter attenuating out of band high frequency interferers before sampling act as an anti-alias filter. The CT sigma delta converters have found in such applications as wireless communications systems, signal processing, readouts powerless biological signal, in micromachined consumer and professional audio, industrial weight scales and precision measurement devices. In this design, a new approach for CT sigma delta modulator, offered new implementation of the active integrator with current conveyor (CCII) is presented [12]. The CCII circuit due to multiple reasons such as low complexity, high bandwidth, linearity and invariant by processes variation effects can be suitable choice for design integrators of the CT sigma delta modulators.

2 Basic principle

Fig. 1 shows the block diagram of a general CT sigma-delta modulator, which consists of a loop filter H(s), non-return to zero (NRZ) D/A and a quantizer. In this modulator the analog input signal is modulated to a digital word sequence with a frequency spectrum that approximates the analog input spectrum in a narrow frequency range, while the quantization noise is shaped away from this frequency range. Using impulse invariant transformation for a second order low-pass loop filter of a sigma-delta modulator H(s), the following transfer function is achieved [4] as:

$$H(s) = \frac{(1+1.5Ts)}{(Ts)^2} = \frac{1}{(Ts)^2} + \frac{1.5Ts}{(Ts)^2} \quad (1)$$

where, T is the period of the sampling.

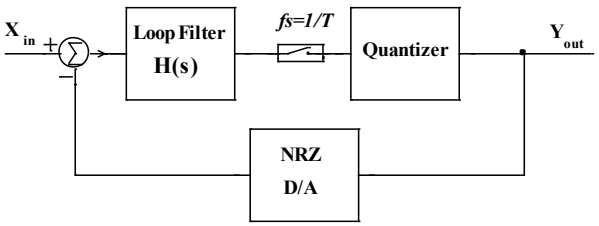

Fig. 1: Block diagram of a CT sigma-delta modulator

3 Circuit design

3.1 Current conveyor

The second generation current conveyor (CCII) is a current mode analog building block which can substitute operational amplifiers in some applications [5,6]. A recent target for CCII is the design of low voltage and low power CCII structures [7], in particular for The CCIIs can be used for varying the range of analog filters, differentiators, integrators, admittance or inductance simulator and oscillators. Fig. 2 shows symbol diagram of a CCII. A CCII has three ports, conventionally referred to as X, Y and Z. Ideally, if a voltage is applied to node Y, the CCII will produce an equal voltage at node X. Also, the current flowing into the node X is copied into the node Z. The function of a CCII± can be described by following equation:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 1 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_x \\ I_x \\ V_z \end{bmatrix} \quad (2)$$

Difference between CCII+ and CCII– is the direction of the current of Z terminal. Fig. 1 shows the circuit symbol of CCII, where Y is voltage input with high input impedance, X is voltage trace terminal, Z is no inverting current output terminal, -Z is inverting current output terminals.

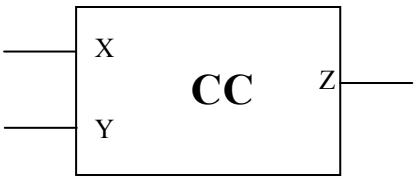

Fig. 2: Symbol diagram of the employed CCII

Fig. 3 shows circuit diagram of the employed CCII that is modified version of the circuit reported in [8]. In this Figure, transistors M6 and M9 forms n-type differential pair of amplifier. Transistors M4 and M5 are the current mirror and the load and transistor M14 is current tail of amplifier. In complementary transistors M7 and M8 employed for p-type differential pair of amplifier and transistors M12 and M13 are the current mirror and the load and transistor M1 is current tail of amplifier. Also, transistors M2, M3, M10, M11, M15 and M16 are used for current mirroring of port X.

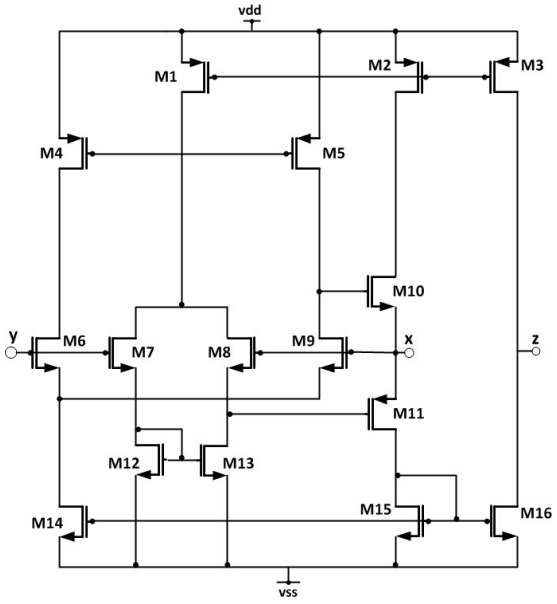

Fig. 3: Circuit diagram of the employed CCII

3.2 Integrator

Fig. 4 shows single ended block diagram of a second order loop filter based on (1). The maison's rule prove this transfer function and design purposed with unit factor feedback loop[4]. To design of the loop filter many proposals such as transconductance and capacitance (gm-C), hybrid active-passive loop filter and switch current is presented [9,10]. In this work, an alternative loop filter based on current conveyors is employed for sigma delta modulators.

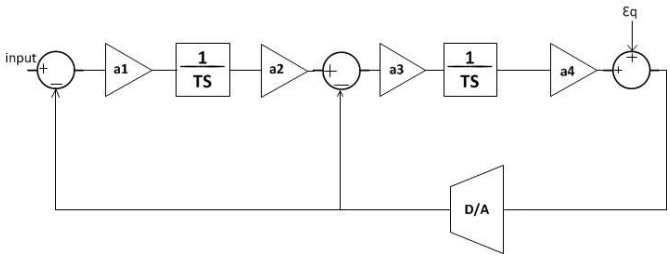

Fig. 4: Block diagram of a second order loop filter

3.3 Quantizer

Fig. 6 shows circuit diagram of the applied quantizer. The quantizer consists of a one bit comparator, followed by a D-latch [11]. Two differential amplifiers with diode loads by transistors M1-M10 are used as pre-amplifier and front-end of comparator. Also cross coupled amplifier as a track-and-latch (by transistors M11-M16) is employed for back-end of clocked regenerative comparator. Fig. 7 shows circuit diagram of D flip-flap that composed by two back-to-back not gate (transistors M1-M4) for memory cell and another not gate for voltage compatibility of the output (transistors M5, M6). CCII as the core and a capacitor and a resistor is employed, which is shown in Fig.

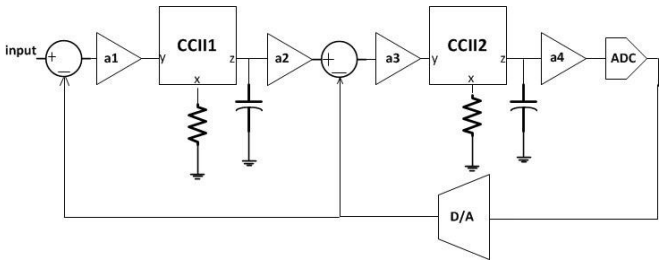

Fig. 5: Block diagram of a second order loop filter using CCII

3.4 DAC

Fig. 8 shows the 1 bit D/A converter that employs two voltage sources and two switches, whose voltages are directed via switches that are controlled by the output of the quantizer. When the switch q turns on, the positive reference voltage connects to the output node and when switch q turns off, the negative reference voltage connects to the output node.

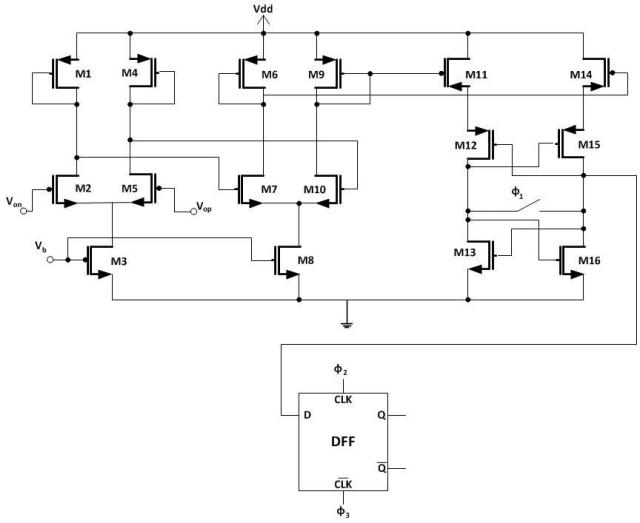

Fig. 6: Circuit diagram of the applied quantizer

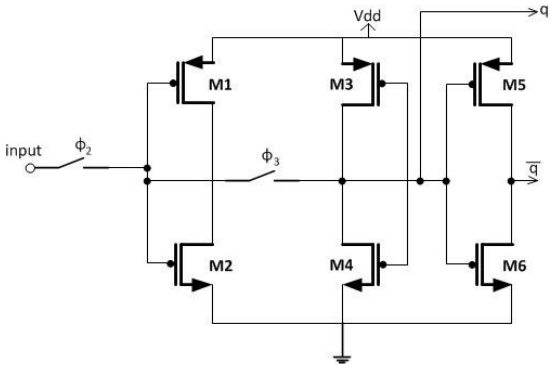

Fig. 7: Circuit diagram of D flip-flap

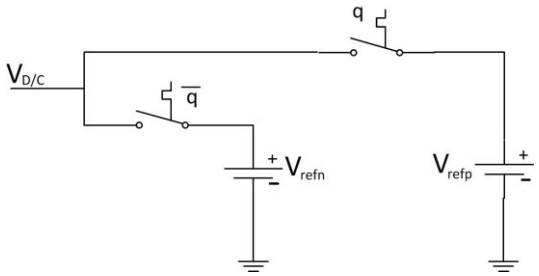

Fig. 8: Circuit diagram of the 1bit D/A converter

4 Simulation results

The proposed second order sigma-delta molulator circuit was simulated by HSPICE in 0.18µm CMOS TSMC technology. R=2.5k, C=20pf, Vdd=1.65V, Vss=-1.65V and Vref=±1V was chosen. Aspect ratios of the NMOS and PMOS of the loop filter were 1u/0.18u, 4µ/0.18µ, respectively and the aspect ratios of the NMOS and PMOS of the quantizer was .3µ/0.18u, .6µ/0.18u respectively. A sinusoidal current input with amplitude of 0.45Vref and frequency of 40KHz was applied for input of modulator. The sampling frequency was set 20MHz the oversampling ratio (OSR), is 64. The output data of the modulator were collected, and then FFT with hanning window was used to evaluate SNR and power spectral density (PSD). Fig. 9 shows the power spectrum of the modulator and Fig. 10 shows Signal-to-Noise vs. input amplitude, which shows that the maximum SNR (including distortion) is 55dB, therefore the bit resolution of proposed modulator is 9bit. Simulation results showed the power consumption of less than 2.8mW. The characteristics of the modulator are summarized in Table I.

5 Conclusion

A new low voltage fully differential sigma-delta modulator based on current conveyors is presented. The circuit employs MOS transistors that operate in saturation region. Simulation results of a modulator show that the technique is promising and can be used in low voltage data converters.

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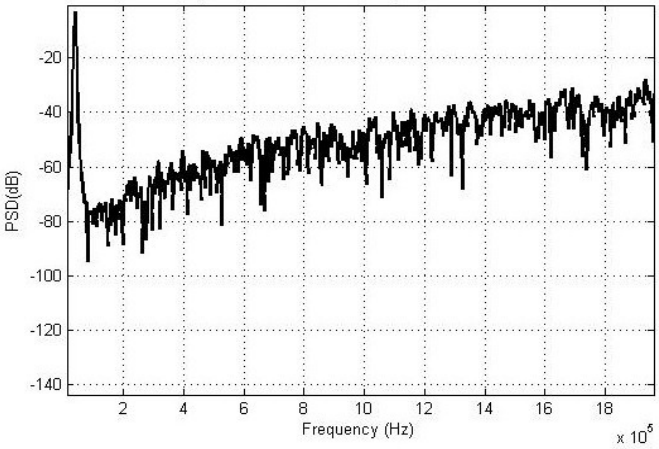

Fig. 9: Power spectrum of the modulator

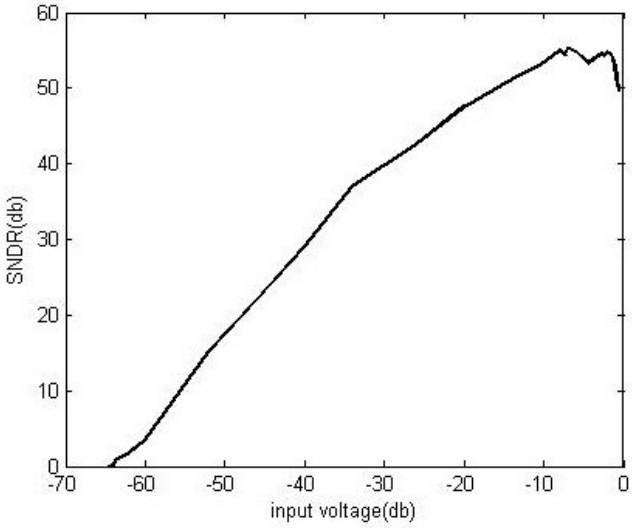

Fig. 10: Signal-to-Noise vs. input amplitude of the modulator

Table I. Circuit Characteristics

Supply voltage	±1.65
Power consumption	2.8mW
technology	0.18µ CMOS
Dynamic range	65db

Sampling frequency	20MhZ
Oversampling ratio	64
Order of loop filter	2
Bit resolution	9bit

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