Proposals for Memristor Crossbar Design and Applications

Memristors and Memristive Systems Symposium
UC Berkeley November 21, 2008

Blaise Mouttet
George Mason University

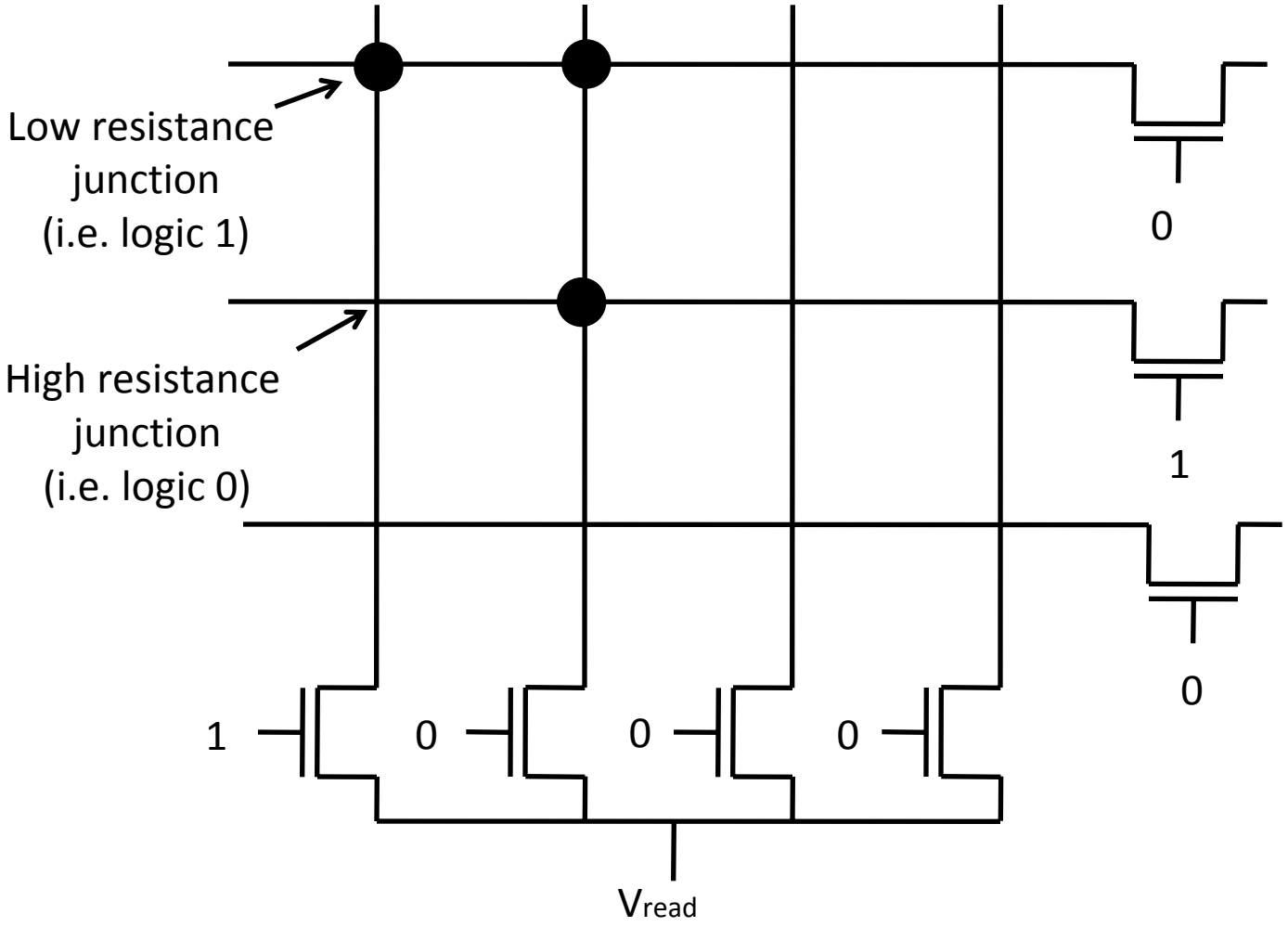
Desirable Manufacturing Goals to Ease Adoption of Memristor Crossbars

- Design should be compatible with standard manufacturing techniques to facilitate wide use and experimentation by many participants (i.e. universities, research labs, existing fabs, etc.) without a significant investment in new equipment.
- Design should be easy to integrate with standard electronics components and materials.
- Design should incorporate materials capable of $R_{HIGH} >> R_{LOW}$.
- Design should be robust to both temporal and spatial variation of memristance.
- Design should avoid internal feedback current paths in crossbar which can limit speed and ability to read resistance states reliably.
- Design should allow ease of reconfiguration of resistance states.

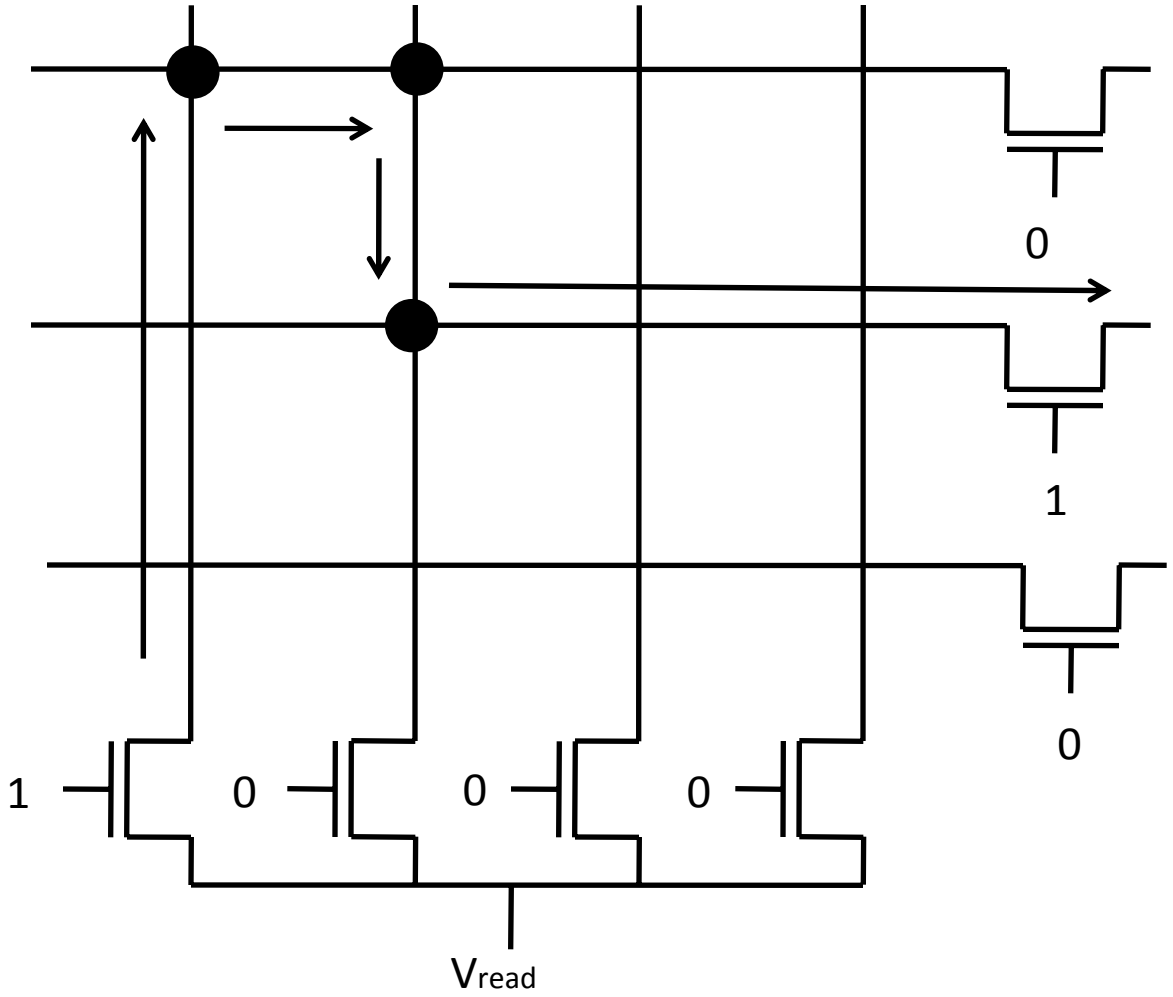
Nanowire vs. Microscale Wire Crossbars

- Some applications may not require nanowires to provide competitive solutions in a variety of areas (e.g. signal processing, pattern recognition)
- Near-term implementation is likely to be easier and more readily adopted using microscale wires which can avoid the problems of nanowire defects, addressing, etc.

Ideally, the detected resistance state of a selected crossbar junction should be independent of other resistance states in the crossbar.

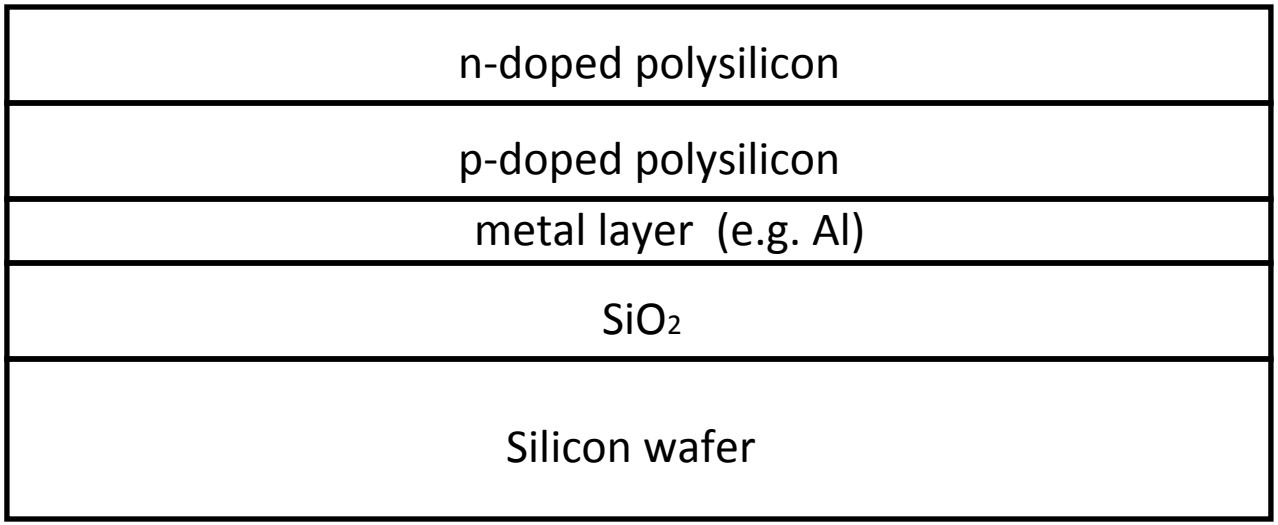


However, this is not the case for simple crossbar designs due to internal currents.

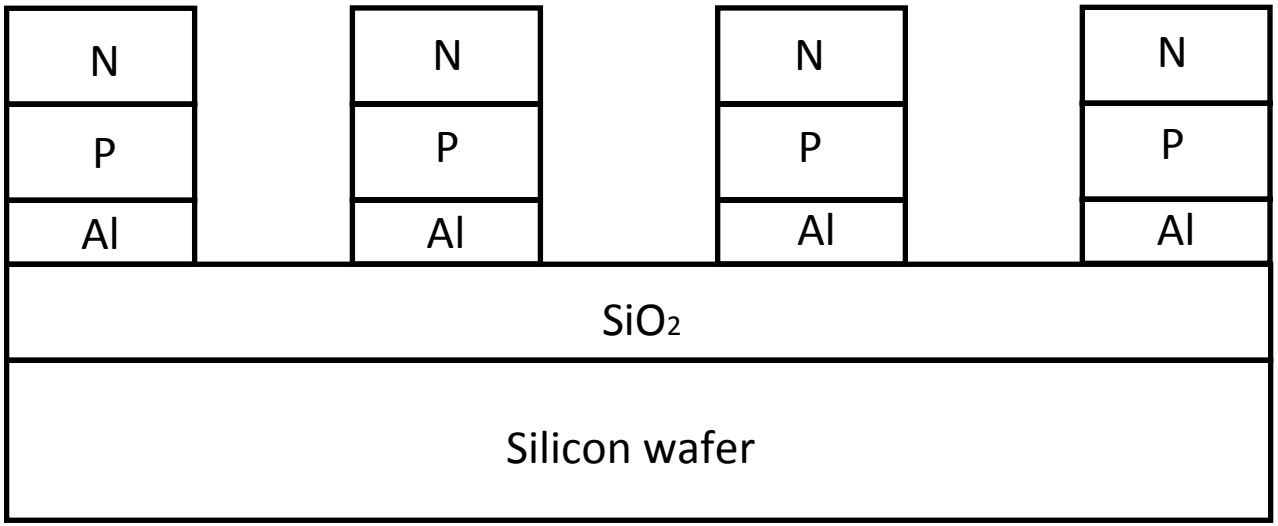


A simple solution compatible with microfabrication techniques is the incorporation of pn junctions in the crossbar (taught by Ovshinsky for phase change crossbar memory in US Patent 4,597,162). One variation of this solution adapted to bilayer oxide memristive films is as follows:

A) Film deposition of metal layer and silicon layers



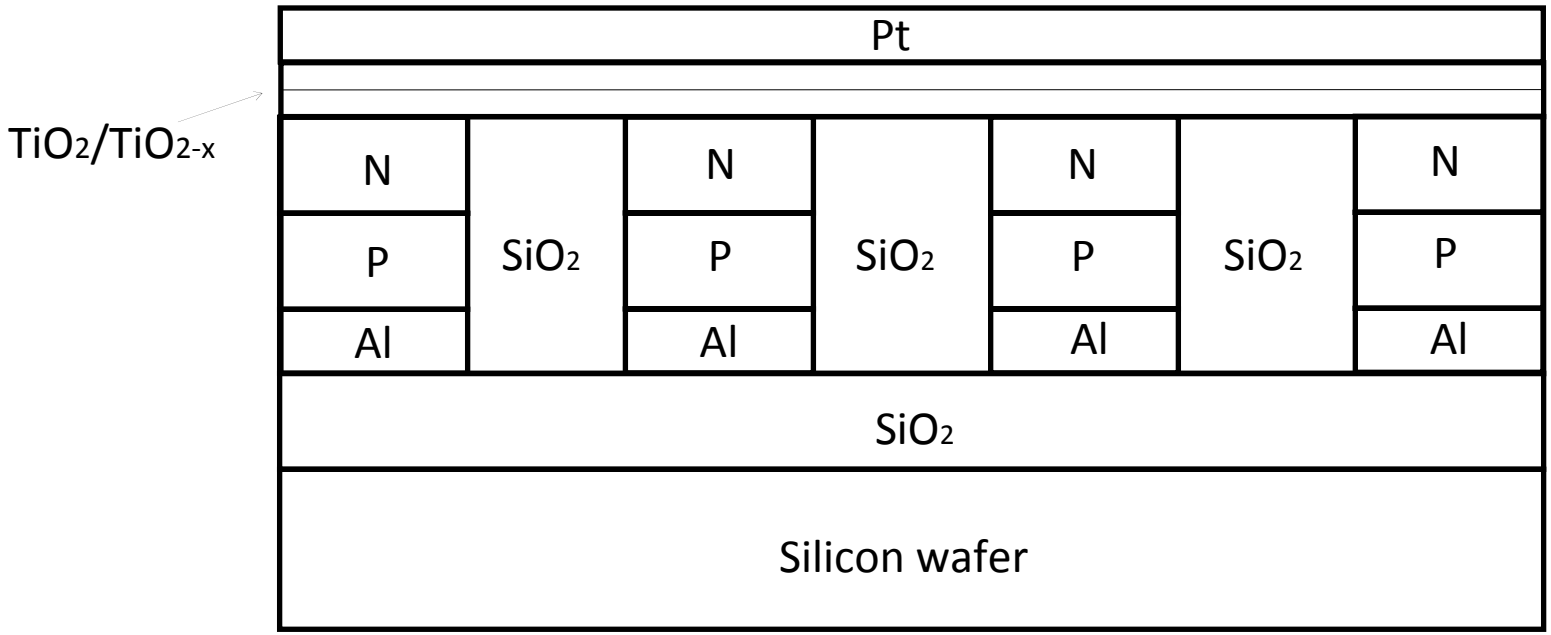
B) Etch metal and semiconductor layers to form crossbar columns.



C) Deposit SiO_2 in gaps to provide isolation and planarize surface

D) Deposit memristor oxide bilayer (e.g. TiO_2/TiO_{2-x})

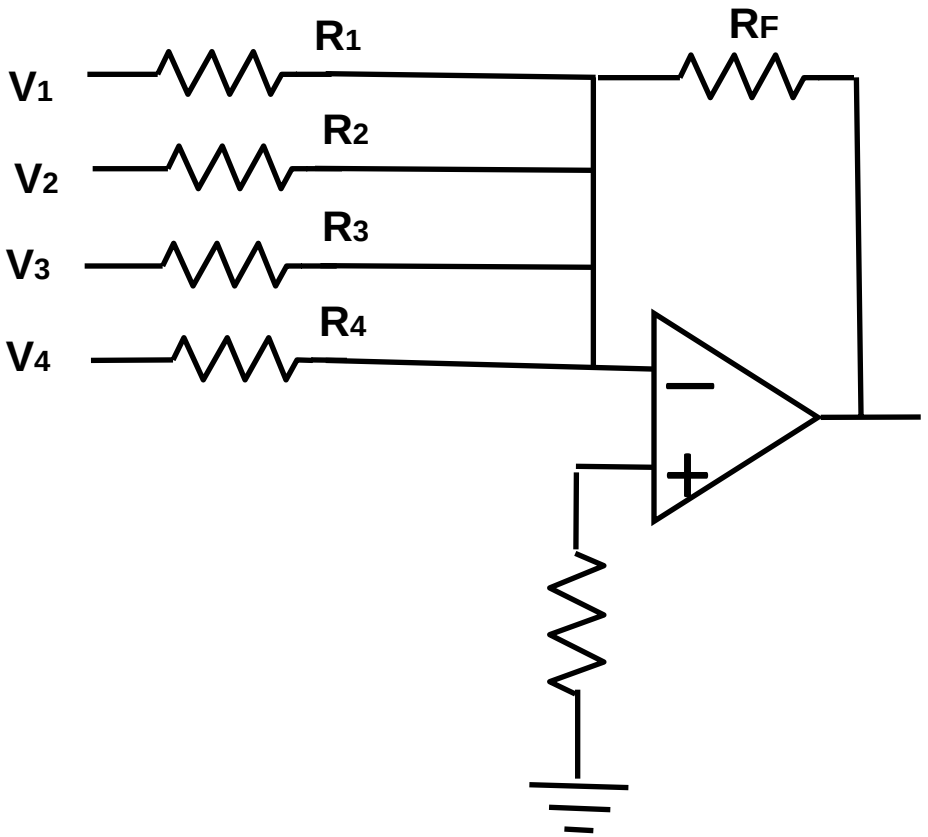
E) Deposit and pattern top metal layer to form crossbar row wires



Desirable Goals for Memristor Crossbar Array Applications

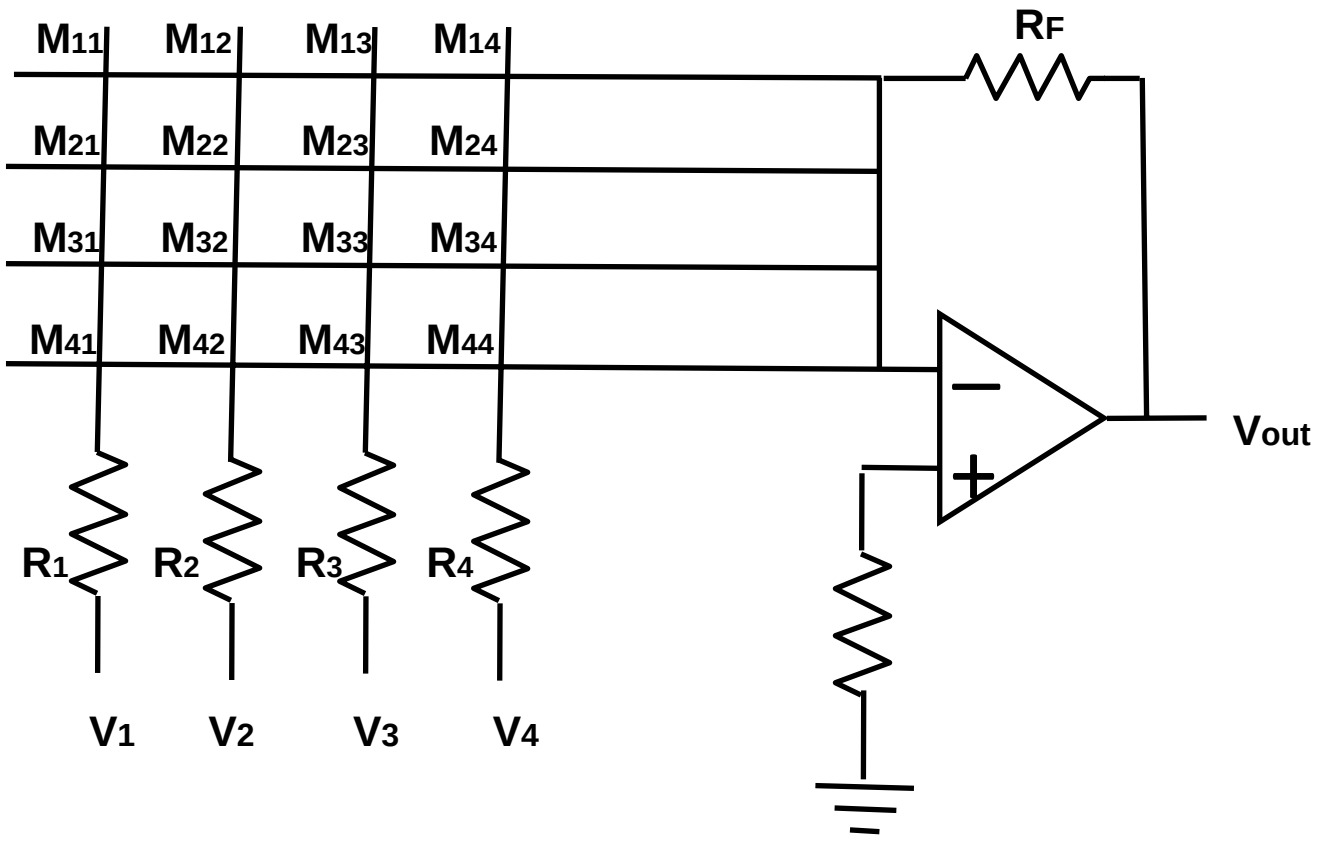
- Complement (not conflicting with) existing technologies and markets to achieve ease of acceptance
- Identify uses compatible with smaller emerging markets with potential for high growth (e.g. FPAAs , commercial robotics, neural interfaces)
- Solve problems for which conventional electronic hardware and software do not provide efficient solutions but which memristors can (e.g. pattern recognition, traveling salesman problem)

Op-amps are well known to be implemented as summing amplifiers



$$V_{out} = -\left[V_1(R_F/R_1)+V_2(R_F/R_2)+V_3(R_F/R_3)+V_4(R_F/R_4)\right]$$

Integrating Memristor Crossbar Array with Op-Amp Circuitry = Matrix Summing Amplifier



For an ideal op-amp:

$$I_F = -\sum_{ij} I_{ij}$$

$$\frac{V_{out}}{R_F} = -\sum_{ij} \frac{(V_i - V_{loss})}{(M_{ij} + R_i)}$$

$$V_{out} = -\sum_{ij} \frac{R_F}{(M_{ij} + R_i)} (V_i - V_{loss}) = -\sum_{ij} T(M_{ij})(V_i - V_{loss})$$

To achieve behavior similar to binary logic requires $T(M_{ij}=R_{HIGH})=0$ and $T(M_{ij}=R_{LOW})=1$

By setting the fixed column resistors $R_i = R_F-R_{LOW}$ then $T(R_{LOW})=1$ is achievable. However, $T(R_{HIGH})$ is not able to be zero since this would require $R_F = 0$. Thus a low bit error (LBE) exists and a tolerable LBE should satisfy:

$$T(R_{HIGH})= LBE \geq 1/[1+(R_{HIGH}-R_{LOW})/R_F]$$

Solving for R_F produces:

$$R_F \leq [LBE/(1-LBE)]\ (R_{HIGH}-R_{LOW})$$

This inequality sets an upper limit to R_F based on a maximum allowable low bit error and the high and low resistance values of the memristor.

Analysis for memristor (M_{ij}) variation

For an allowable bit sensitivity $\sigma(M_{ij})$,

$$d\,|T(M_{ij})| = \frac{R_F\, dM_{ij}}{(M_{ij} + R_i)^2} < \sigma(M_{ij})$$

The maximum allowable value of $d|T(M_{ij})|$ is at $M_{ij} = R_{LOW}$ and for $R_i = R_F - R_{LOW}$

$$\frac{R_F\, dM_{ij}}{(R_{LOW} + R_F - R_{LOW})^2} = \frac{dM_{ij}}{R_F} < \sigma(M_{ij})$$

Analysis for memristor (M_{ij}) variation

Combining the previous conditions the optimum range for R_F can be determined based on the memristance sensitivity and low bit error as:

$$\frac{dM_{ij}}{\sigma(M_{ij})} < R_F < \frac{LBE}{1-LBE}(R_{HIGH} - R_{LOW})$$

Analysis for memristor (M_{ij}) variation

A possible rule of thumb is to set the allowable low bit error and bit sensitivity in terms of the number of columns of the crossbar (=N). For example, if all of the crosspoints have a low bit error and sensitivity of 1/N a total of 1 bit error is produced at the output. The range of R_F may then be expressed as:

$$NdM_{ij} < R_F < \frac{1/N}{1-1/N}(R_{HIGH} - R_{LOW})$$

Analysis for memristor (M_{ij}) variation

For large N the above inequality can be approximated to find the maximum allowable variation in M_{ij} as:

$$dM_{ij} < \frac{(R_{HIGH} - R_{LOW})}{N^2}$$

In case of relaxing the maximum bit error and sensitivity constraints to allow for n total bit errors for N columns the above equation becomes:

$$dM_{ij} < \frac{n^2(R_{HIGH} - R_{LOW})}{N^2}$$

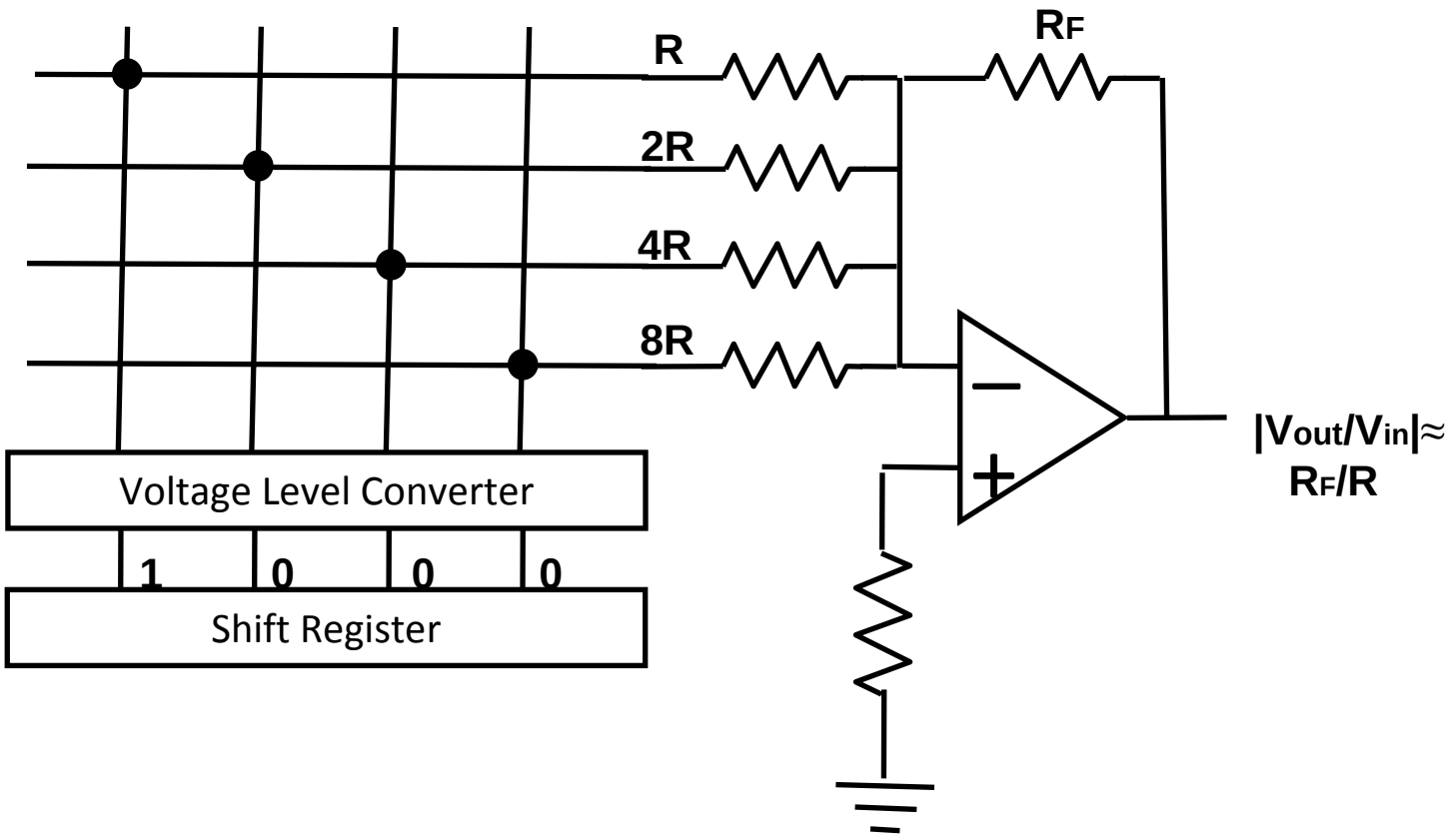
Potential Application #1
Programmable Drive Waveforms

Problems with Conventional Drive Waveform Circuits

- In many electronics applications variation of circuit parameters due to temperature change, aging, etc. require adjustment of drive waveforms (e.g. LEDs may require a higher amplitude voltage drive over time to produce a consistent light output).
- Waveform adjustment is also desirable for mode adjustment in various applications (e.g. inkjet printheads changing resolution or drop size often involves timing or amplitude adjustment of drive signal for heater or piezo.)
- Timing modulation and amplitude modulation circuits implemented in hardware can require complex circuitry and have limitations in adaptability and the range of possible waveforms.
- Software based solutions require a microprocessor which can be difficult/expensive to miniaturize for several portable electronics applications

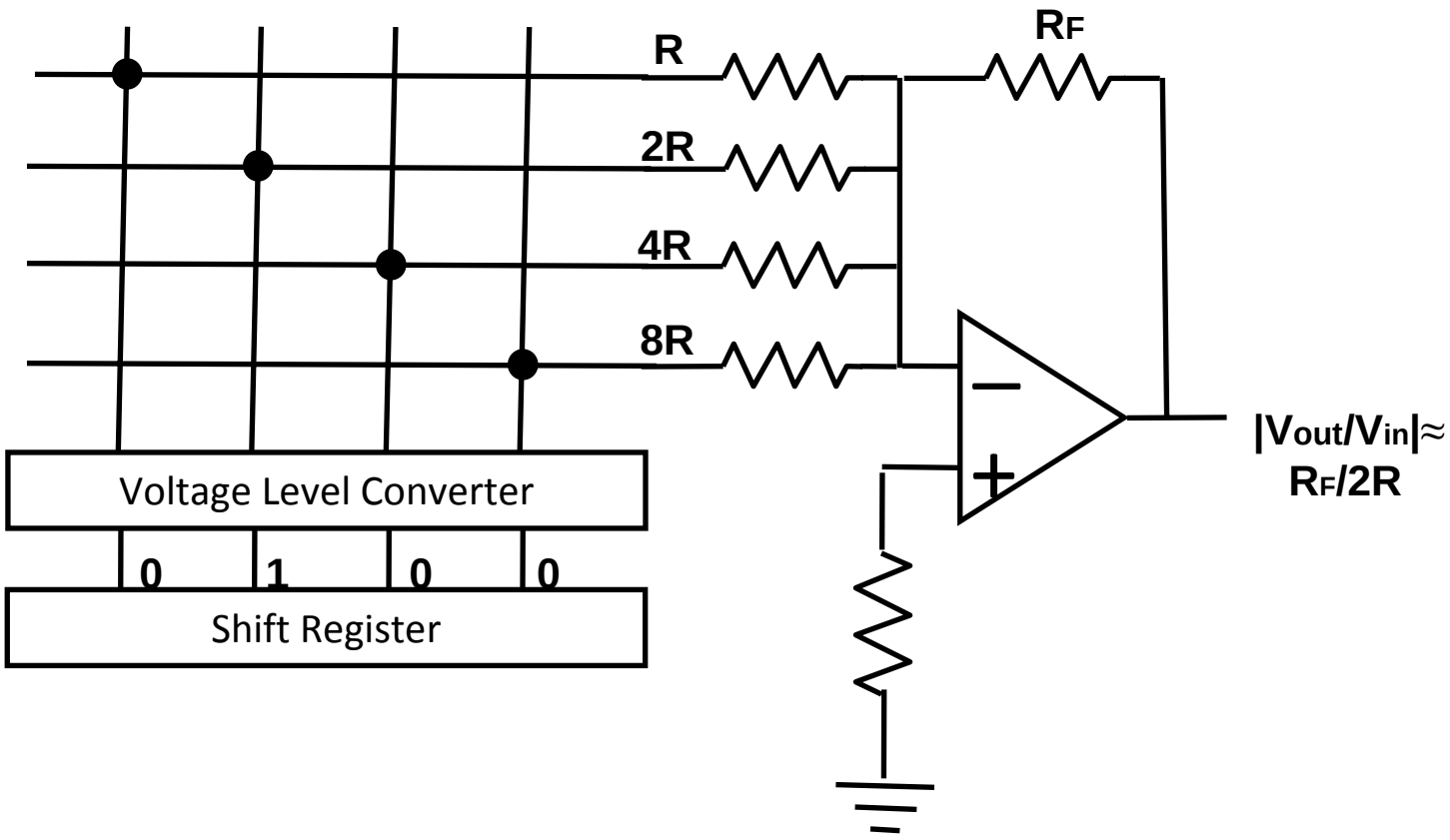
Memristor Crossbar Drive Waveform Circuit

Assuming R_{LOW} of memristors << R_F, R



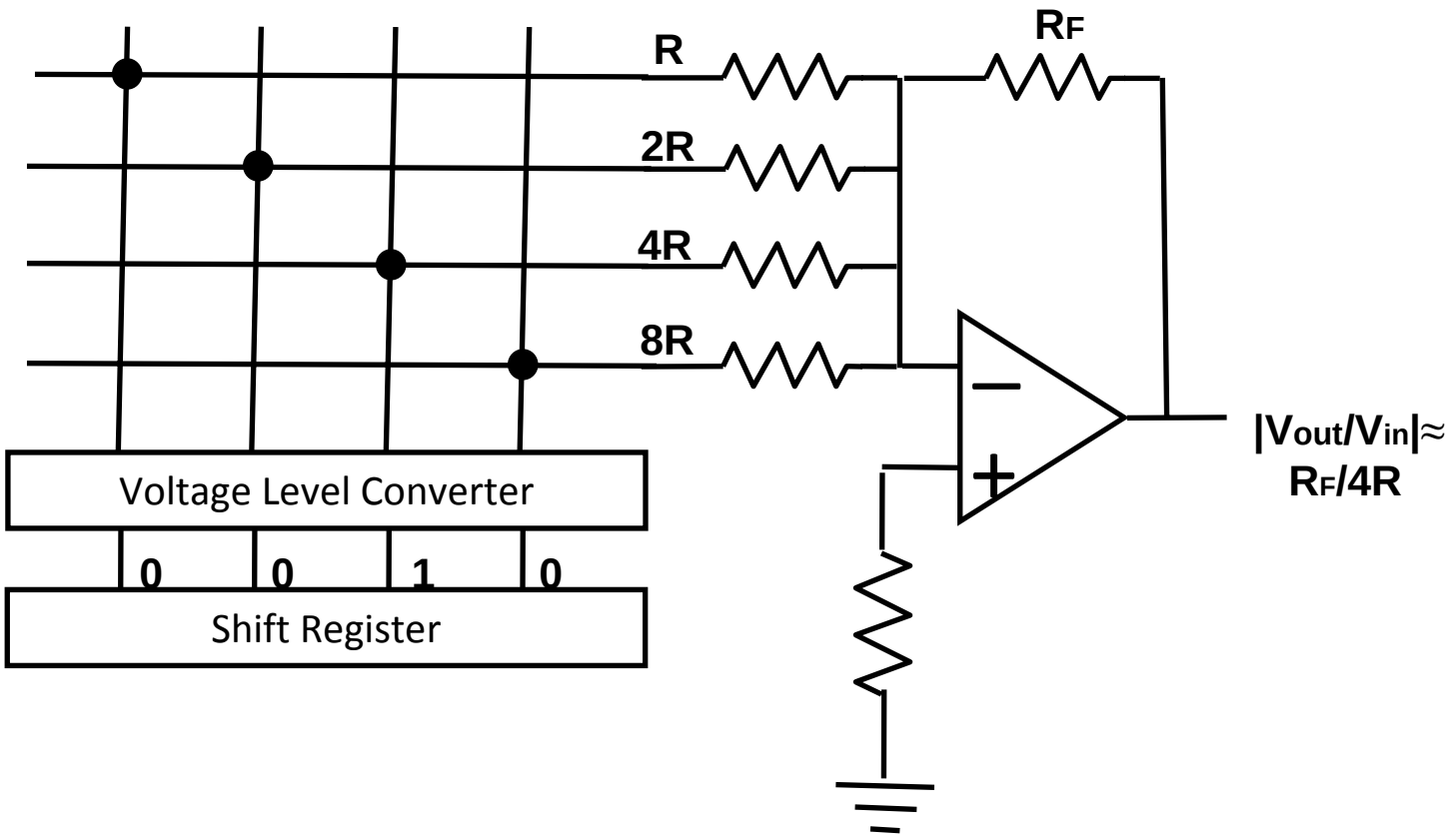
Memristor Crossbar Drive Waveform Circuit

Assuming R_{LOW} of memristors << R_F, R



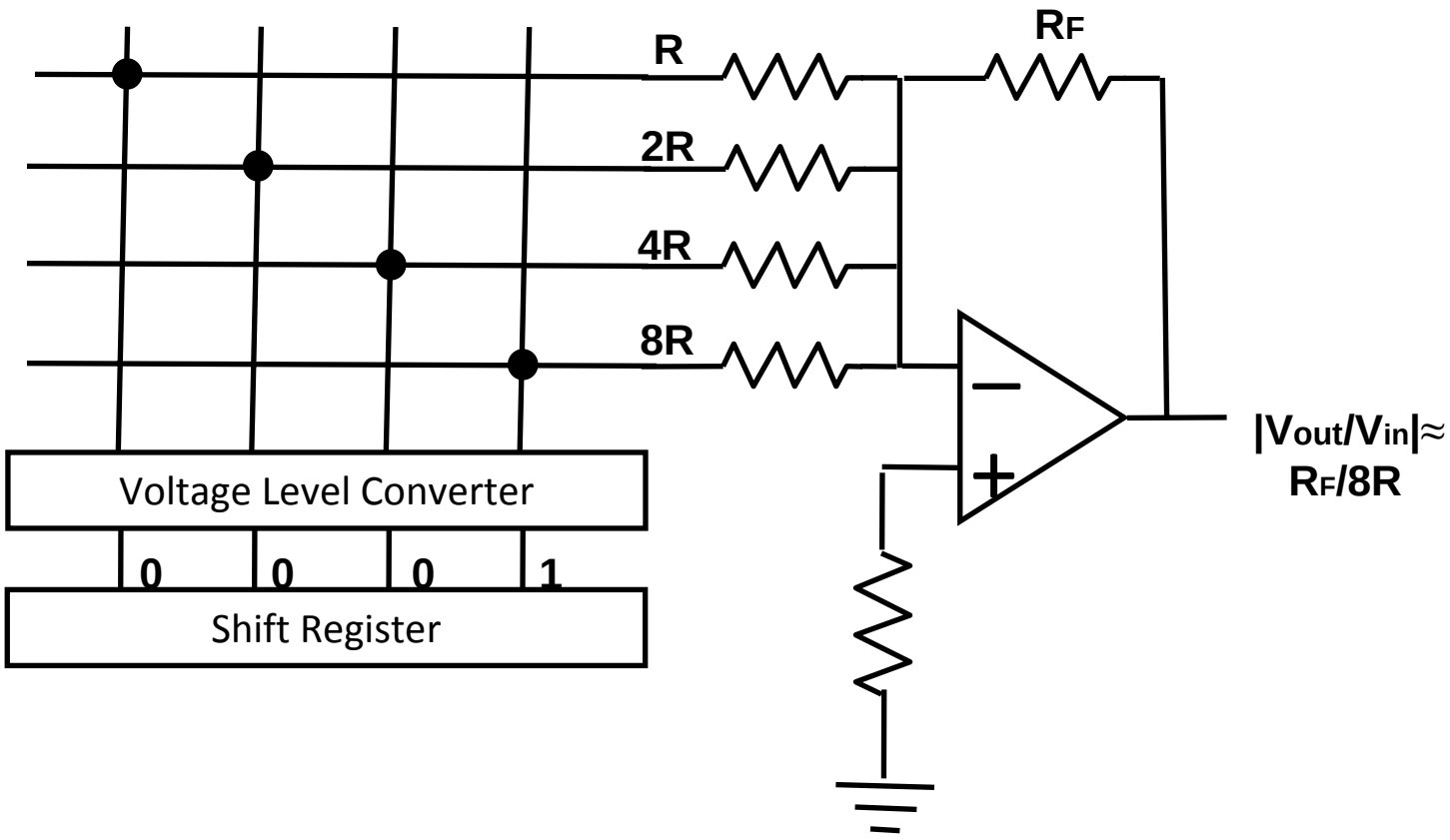
Memristor Crossbar Drive Waveform Circuit

Assuming R_{LOW} of memristors << R_F, R



Memristor Crossbar Drive Waveform Circuit

Assuming R_{LOW} of memristors << R_F, R



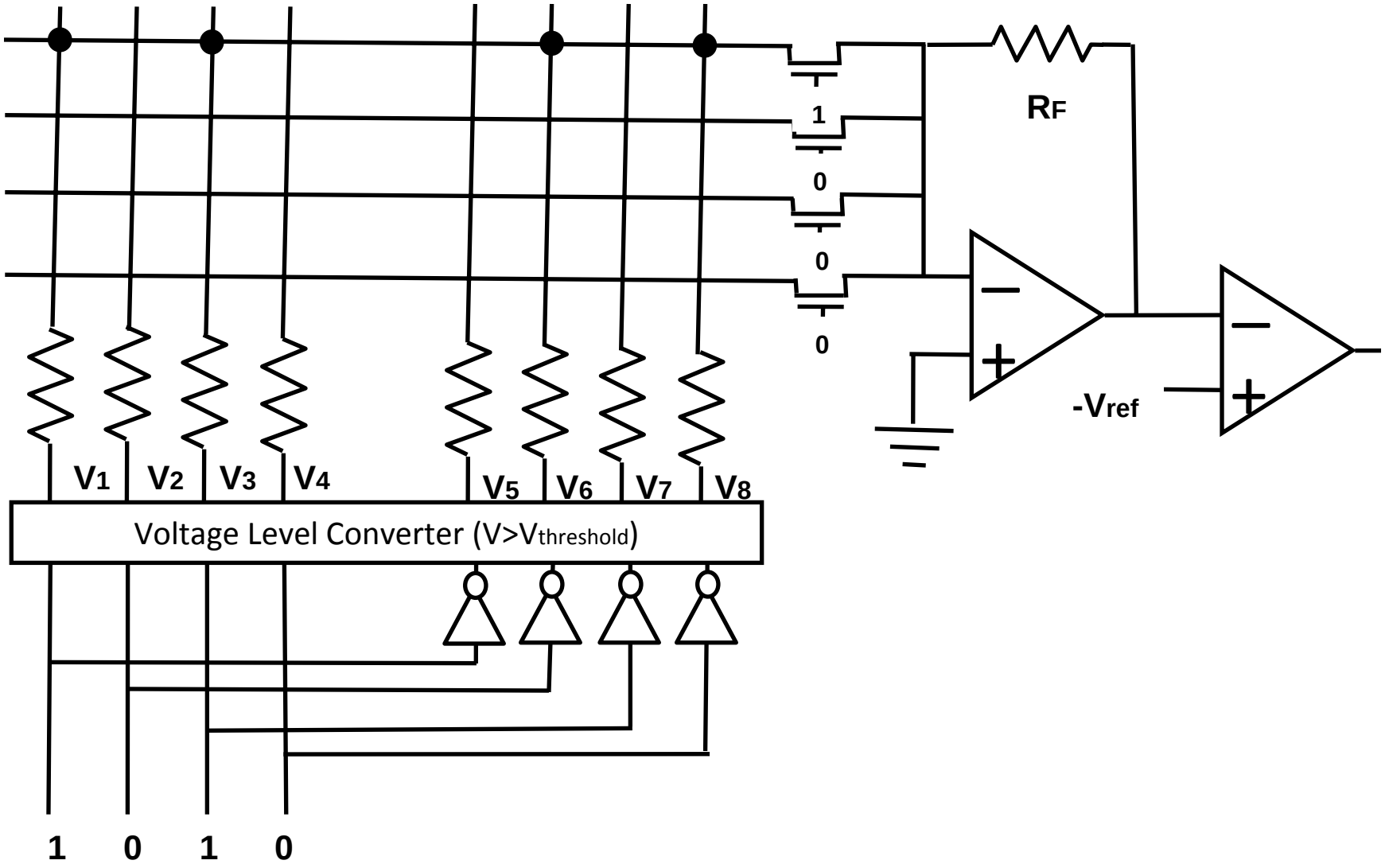
Advantages

- Both timing and amplitude of output waveform can be adjusted by binary switching of the memristance states in the crossbar.
- Even with only binary memristance switching, a very large number of possible drive waveforms are available (2^{NxM}) (e.g. 10x10→10^{30} states).
- Combined with techniques such as hill climbing and genetic algorithms has potential for self-optimizing drive waveforms and real-time adaption of circuitry to effects of aging and temperature variation.

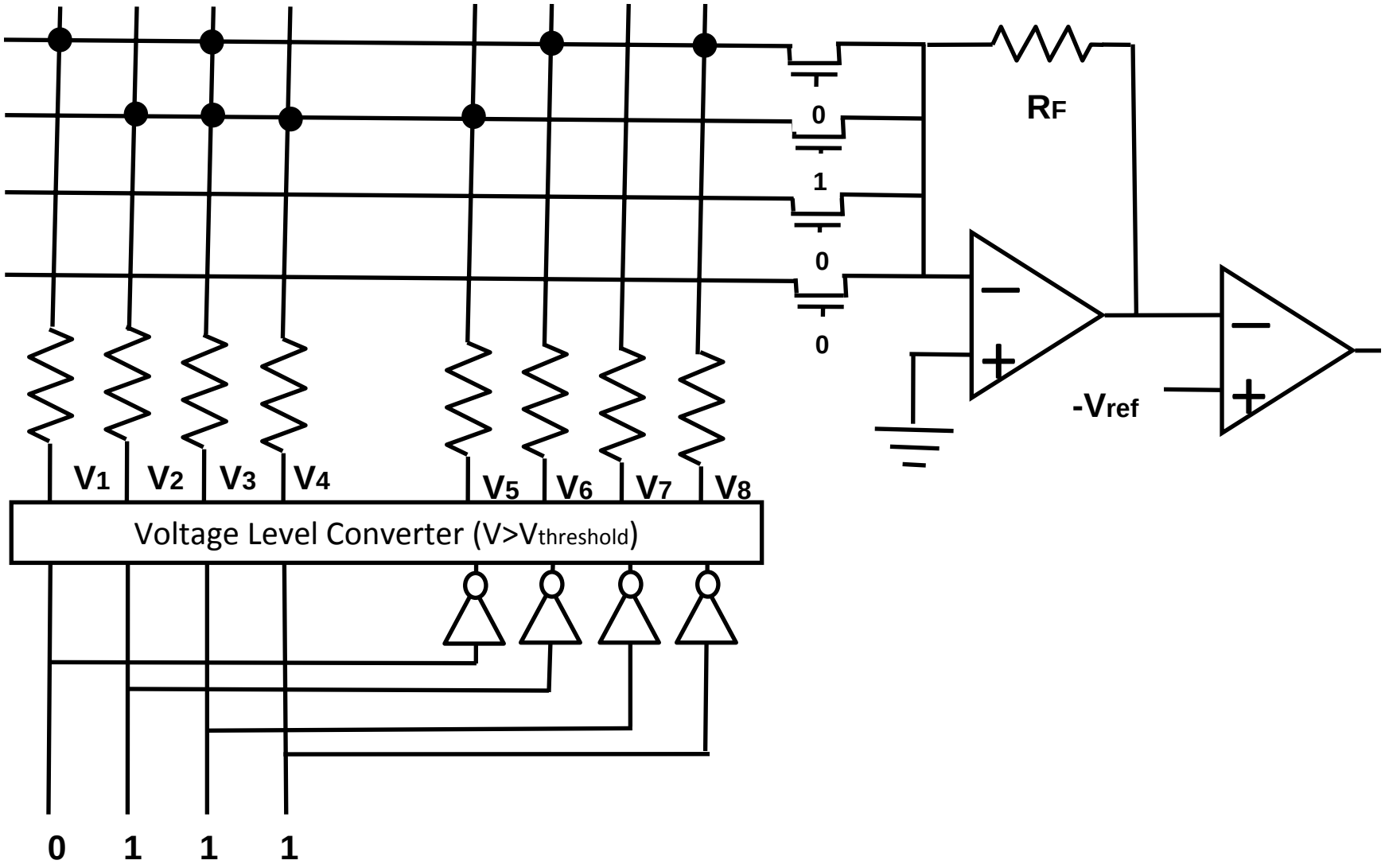
Potential Application #2
Pattern Recognition

Problems with Conventional Pattern Recognition Solutions

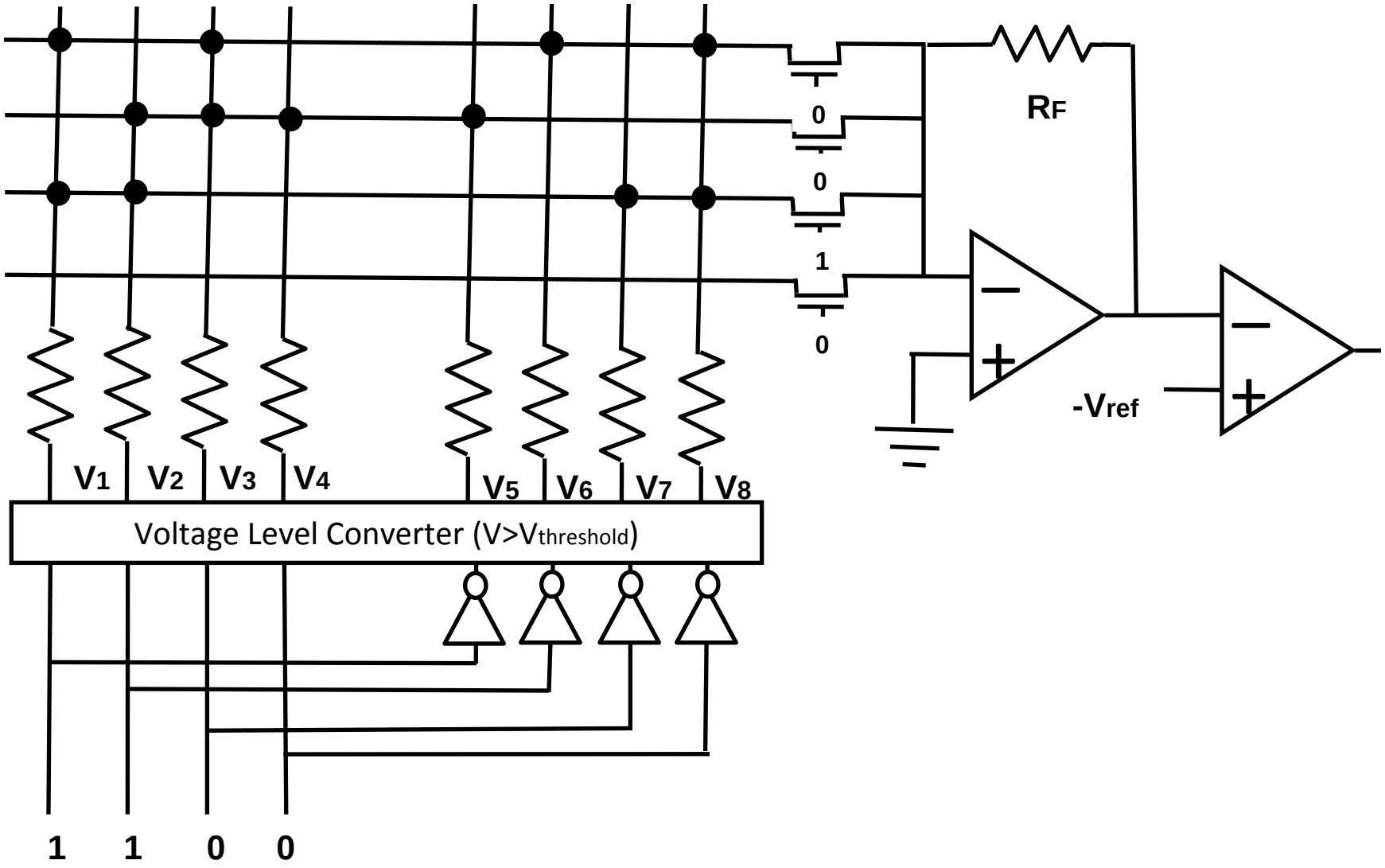
- Software-based solutions require time for data transfer between memory and processor circuits which causes a lag in responsiveness.
- Hardware solutions can be faster but have limits in adaptability and limits in the range of patterns that can be classified.
- Memristors offer a route to a “morphware” pattern recognition solution combining both memory storage and data processing in a common circuit.



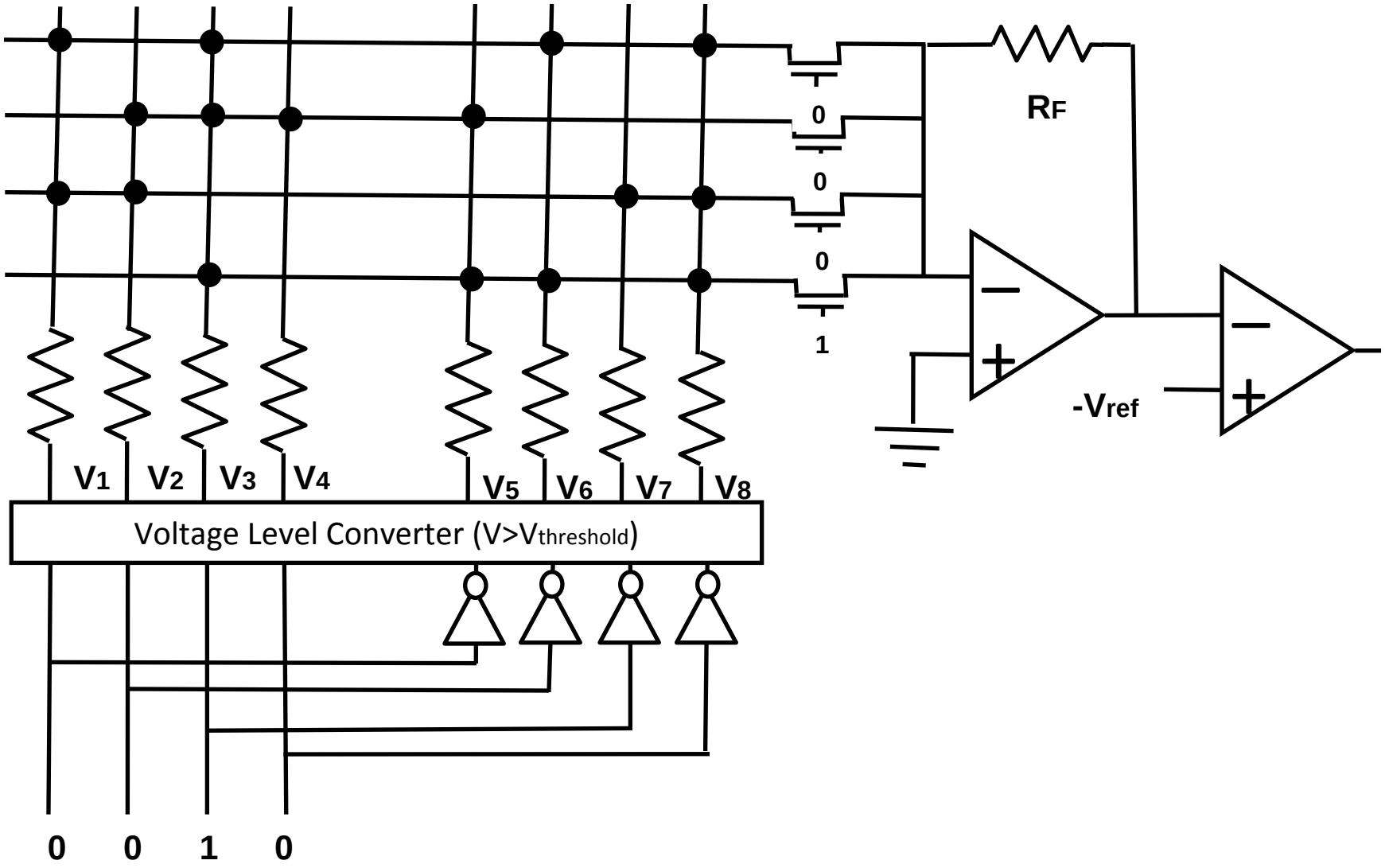
Memristor Crossbar Pattern Comparison Circuit (write mode)



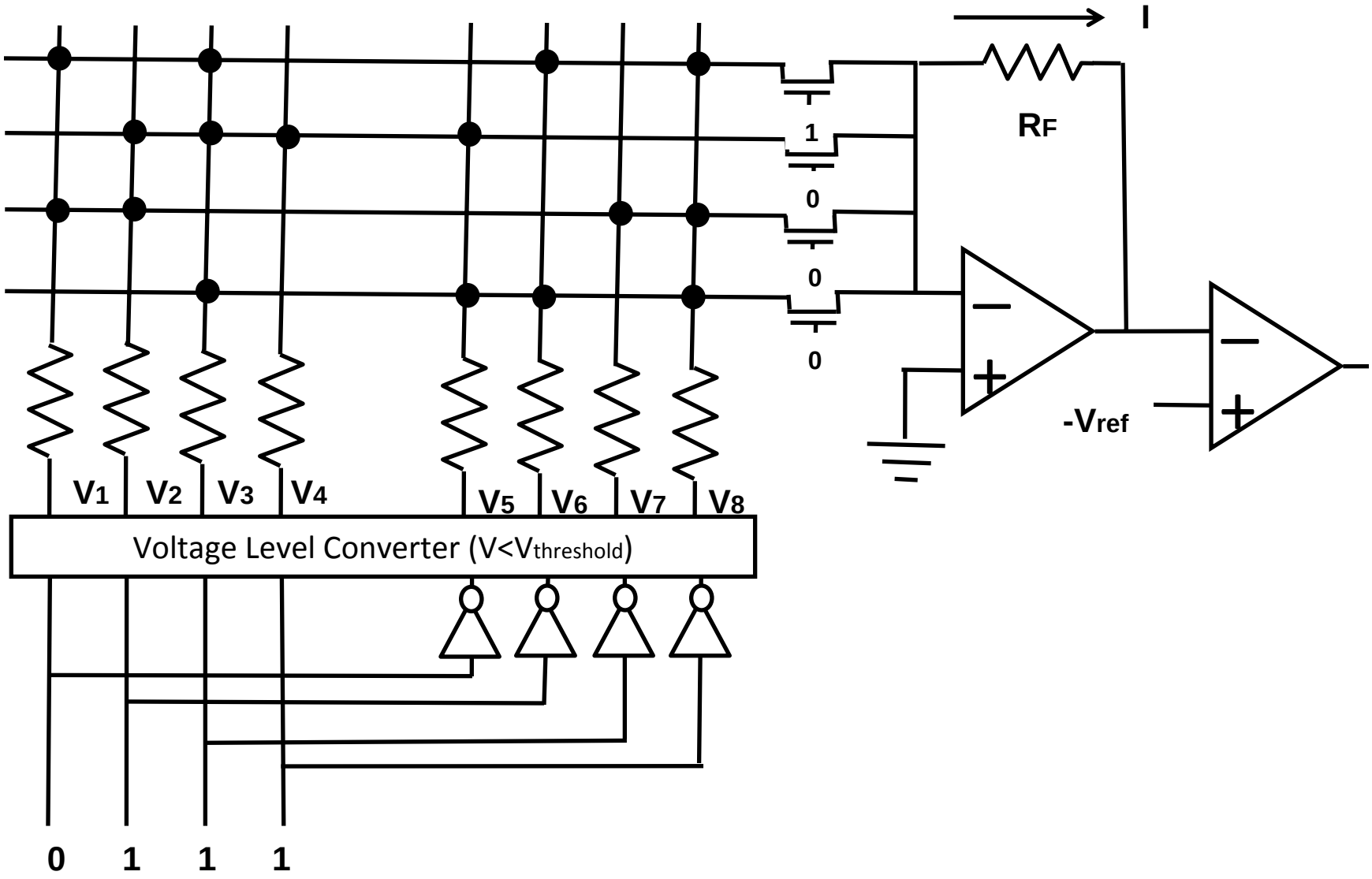
Memristor Crossbar Pattern Comparison Circuit (write mode)



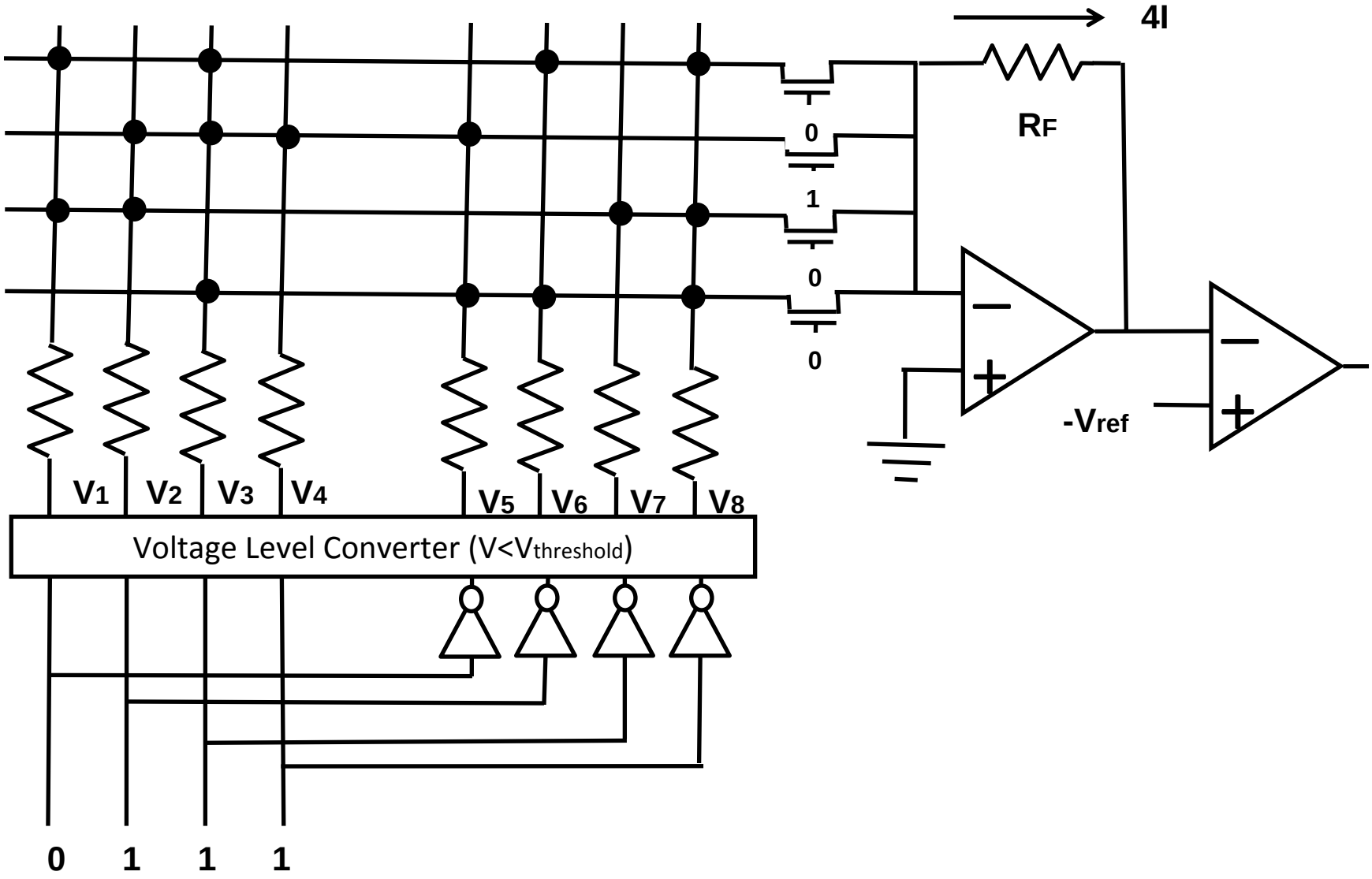
Memristor Crossbar Pattern Comparison Circuit (write mode)



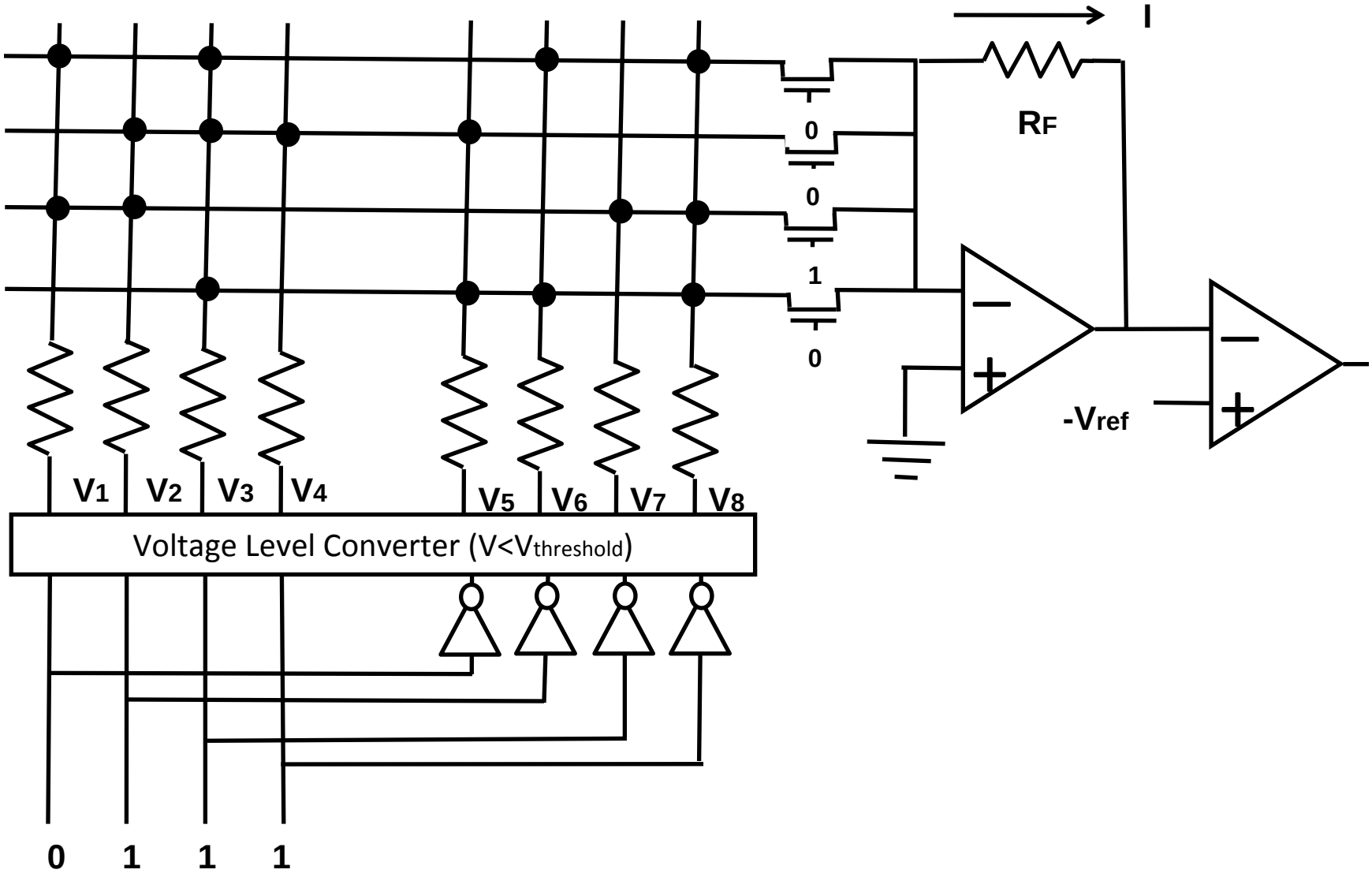
Memristor Crossbar Pattern Comparison Circuit (write mode)



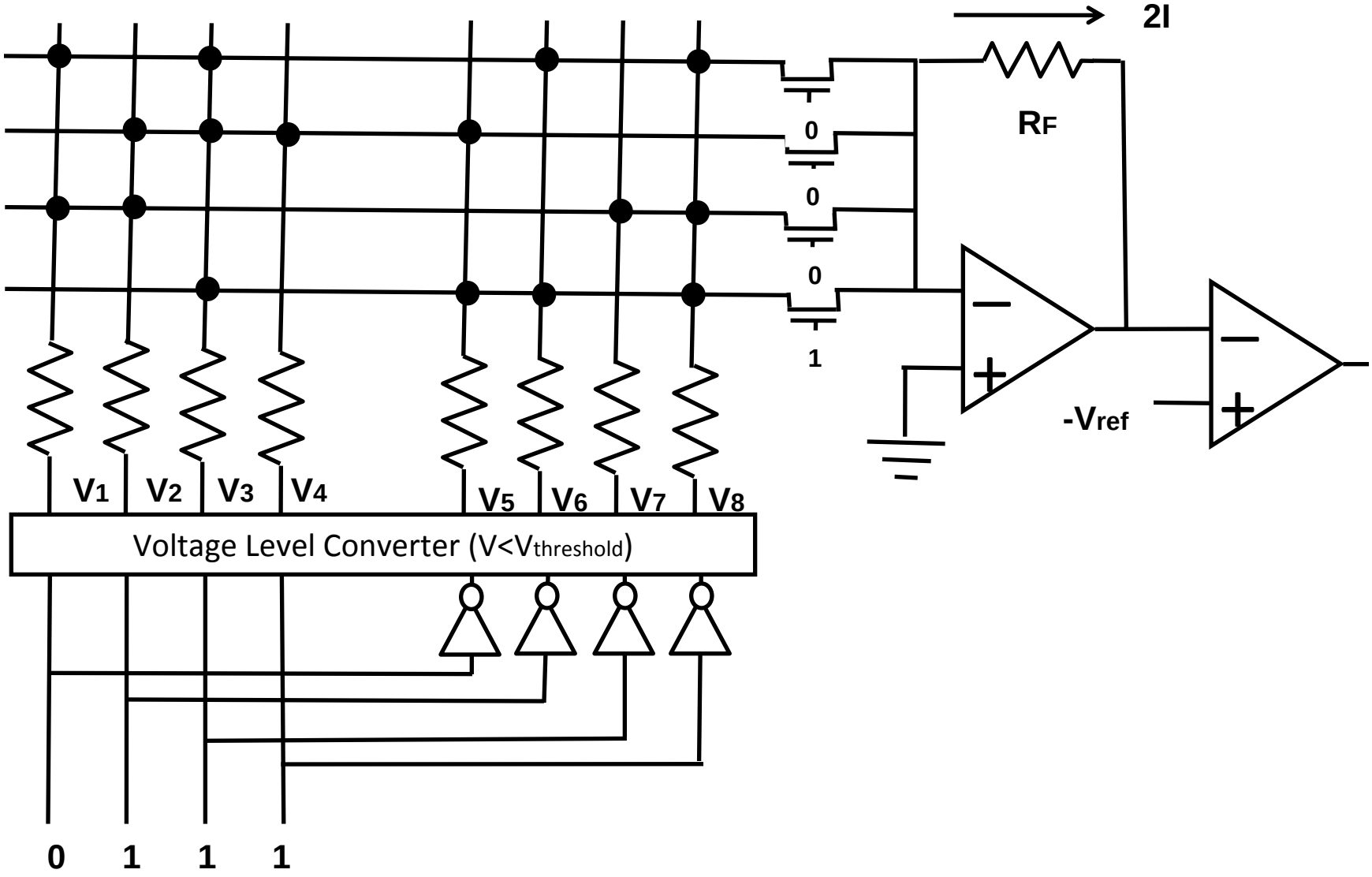
Memristor Crossbar Pattern Comparison Circuit (detect mode)



Memristor Crossbar Pattern Comparison Circuit (detect mode)



Memristor Crossbar Pattern Comparison Circuit (detect mode)



Memristor Crossbar Pattern Comparison Circuit (detect mode)

Advantages

- Output voltage from 1st op-amp is analogous to XNOR (bit comparator) function

$$V_{out\,2} = A([\sum_i T(M_{ij})(V_i - V_{loss}) + \sum_i \overline{T(M_{ij})}(\overline{V_i - V_{loss}})] - V_{ref})$$

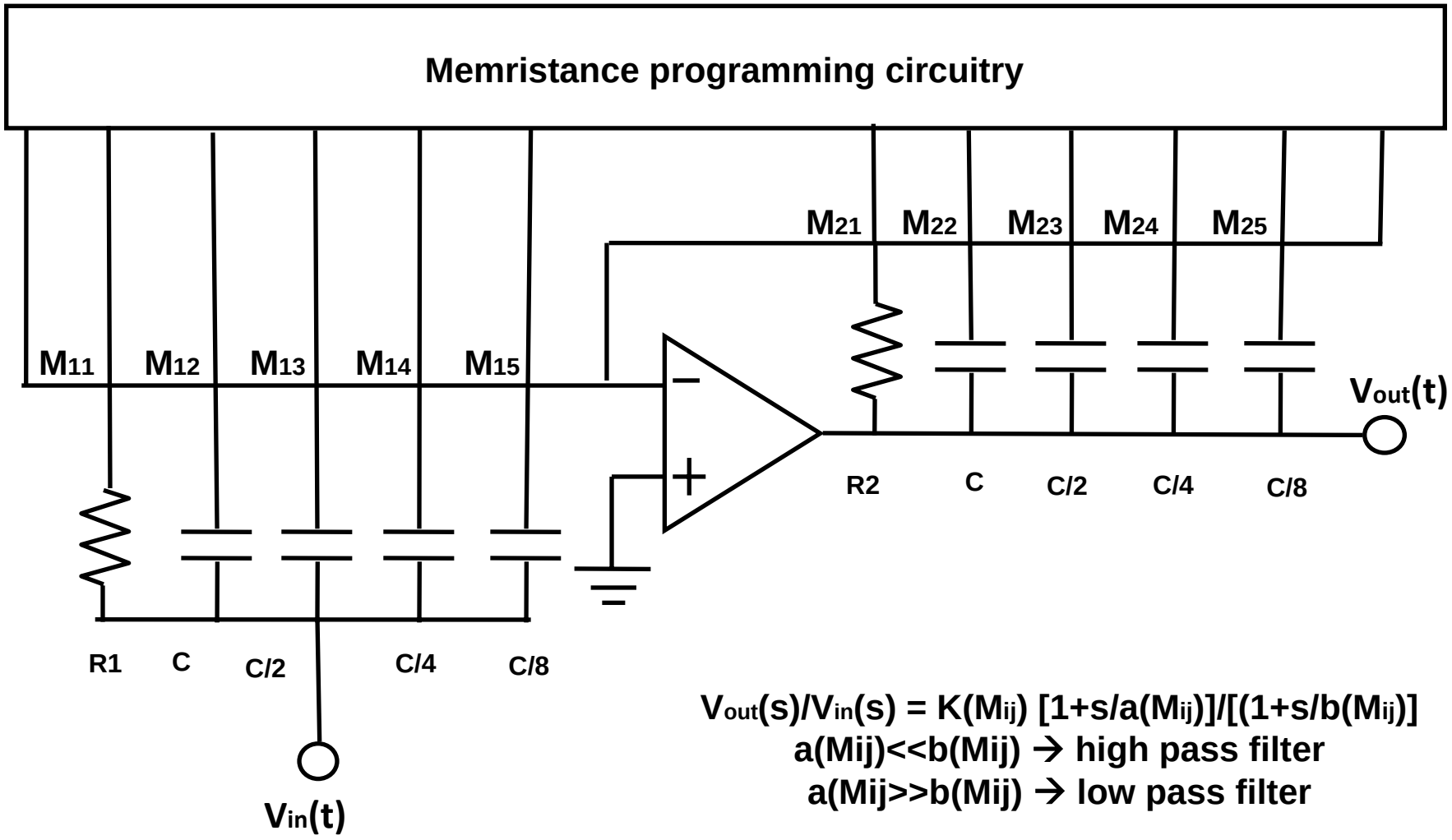
- Tuning V_{ref} can adjust sensitivity of pattern comparison and adjust allowable bit error between resistance states and voltage states.
- Allowing for bit error could potentially be very useful to applications such as facial recognition which can require robustness to a large percentage of bit errors.

Potential Application #3
FPAAs

Problems with Conventional FPAAs

- FPAAs (Field Programmable Analog Arrays) provide reconfigurability of filter designs useful in communications and control systems but are limited in the range of configurable states.
- Lacks ability to electrically tune the resistance such as provided by memristors to achieve intermediate frequency states (for communication apps.) or pole/zero adjustment (for control apps.)

By including memristor crossbar junctions in the input and feedback path of an op-amp capacitor array, a transfer function can be tuned to adjust the gain, pole, and/or zero of a filter.



$V_{out}(s)/V_{in}(s) = K(M_{ij})\,[1+s/a(M_{ij})]/[(1+s/b(M_{ij})]$

a(Mij)<<b(Mij) → high pass filter

a(Mij>>b(Mij) → low pass filter

Advantages

- Conversion between low pass and high pass filter by appropriate selection of on/off states of M_{ij}.
- Tuning of f_{-3dB} or pole/zero by adjustment of memristance state.
- Cascading multiple stages can provide for tunable bandpass adjustment
- Dynamic PID controllers can be implemented by connecting multiple stages in parallel.

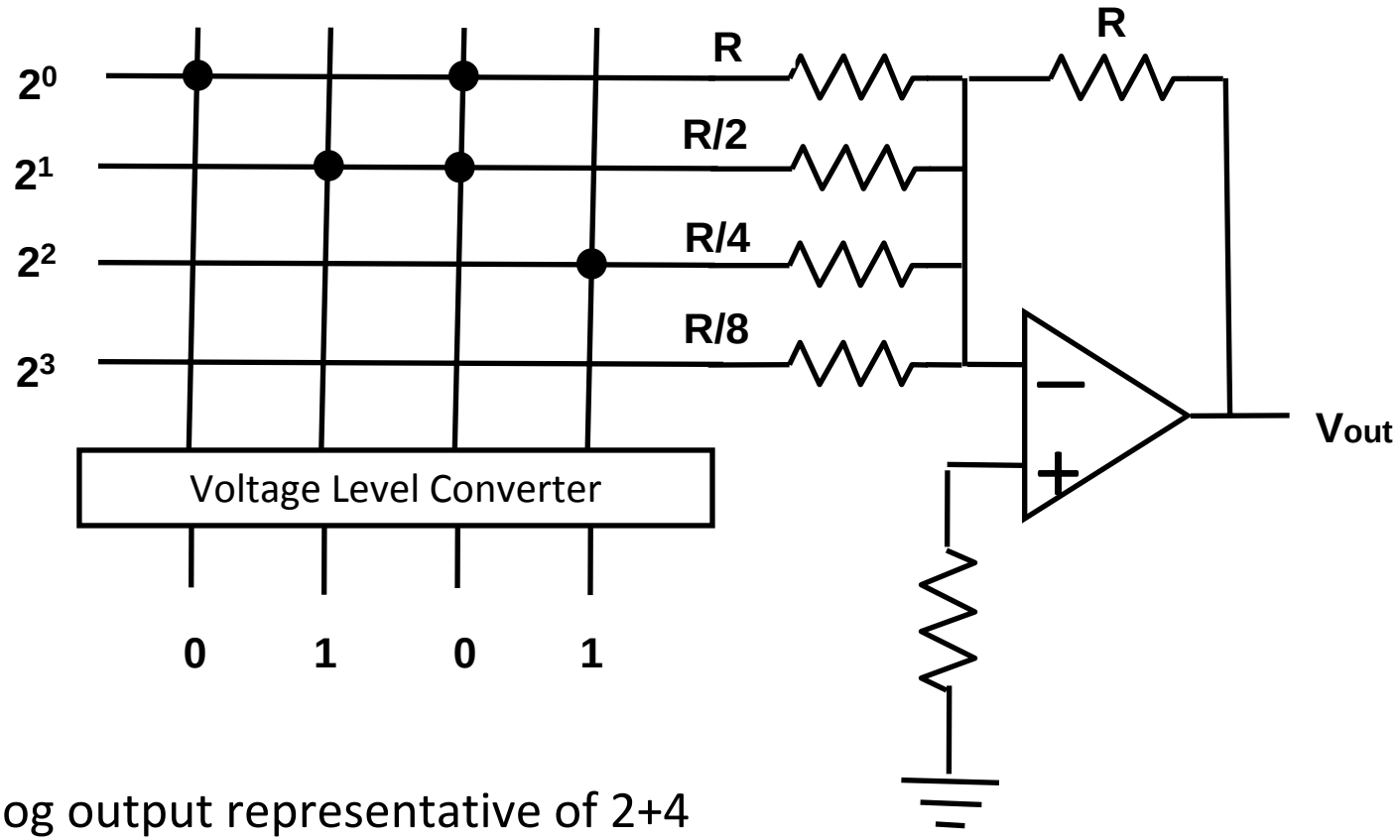
Potential Application #4
Arithmetic Optimization Problems

Problems with Conventional Arithmetic Processor Designs

- Segmentation between memory and processor circuitry may produce a bottleneck in speed. New clock independent designs are desirable.
- Logic based arithmetic is inefficient for some network optimization problems such as the traveling salesman problem involving repeated recalculation of sums

Memristor Crossbar Arithmetic Circuit

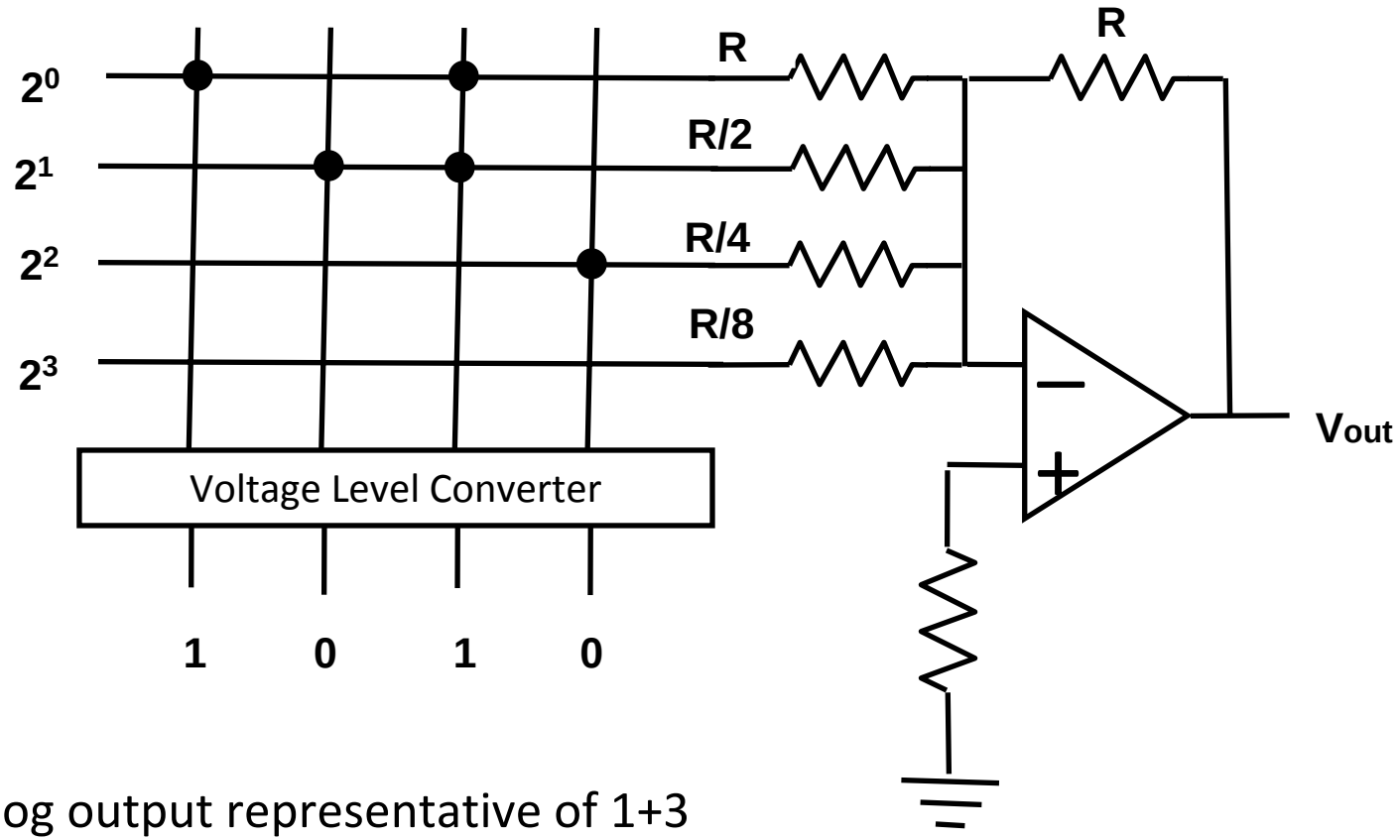
Assuming R_{LOW} of memristors << R/8



Analog output representative of 2+4

Memristor Crossbar Arithmetic Circuit

Assuming R_{LOW} of memristors << R/8



Analog output representative of 1+3

Advantages

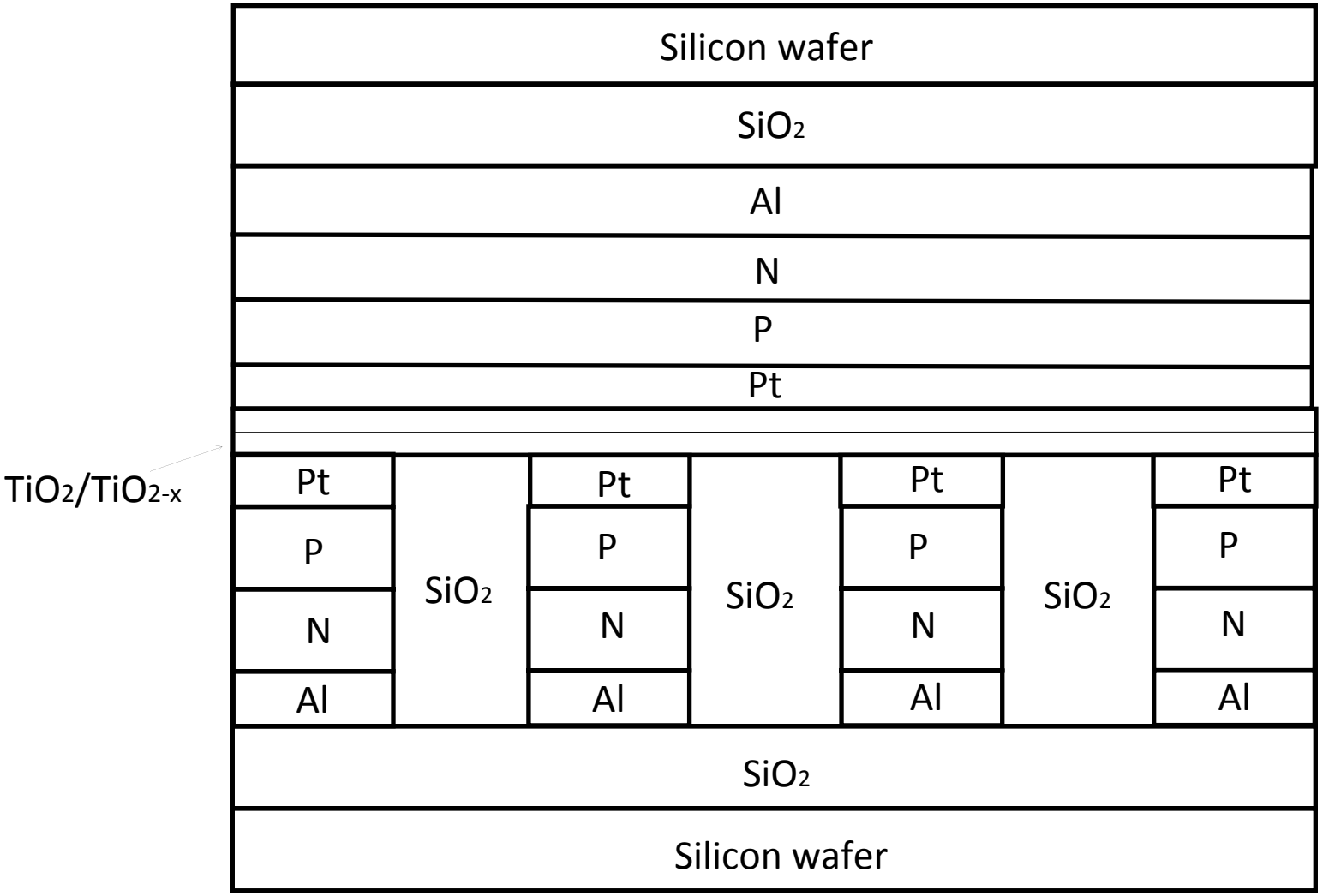
- Although op-amps are slower than logic circuits the combination of memory and processing in a single circuit reduces the reliance on a clock.
- May be scalable to provide real time solutions to network optimization. For example, in a traveling salesman problem with 100 nodes including 5050 inter-relational distances, each distance metric can be stored in a different crossbar column. Comparisons between different paths between the nodes only requires changing the bit pattern input to the crossbar rows and detecting the analog level of voltage output.

Potential Application #5
Signal Mixing

Problems with Conventional Modulation Systems

- Increase in portable wireless electronics requires more efficient uses of spectrum with techniques such as frequency hopping.
- Simpler but more secure signal encryption methods are desirable.

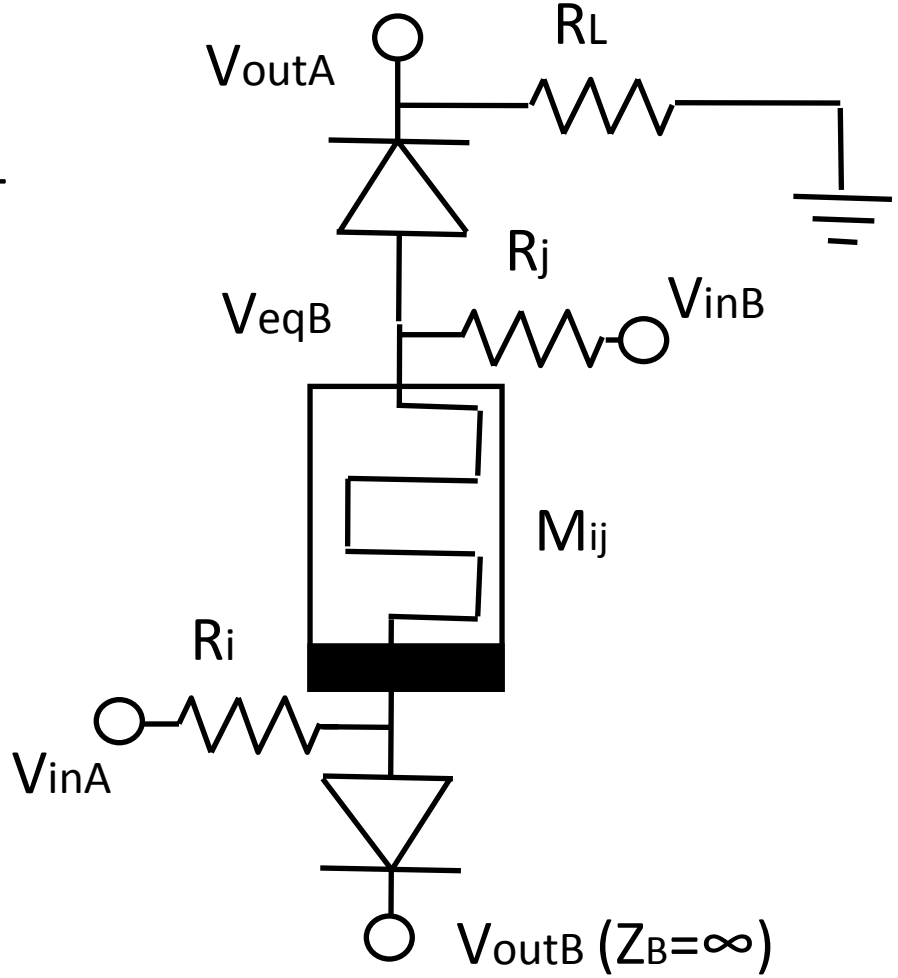
Back-to-back diode memristor crossbar



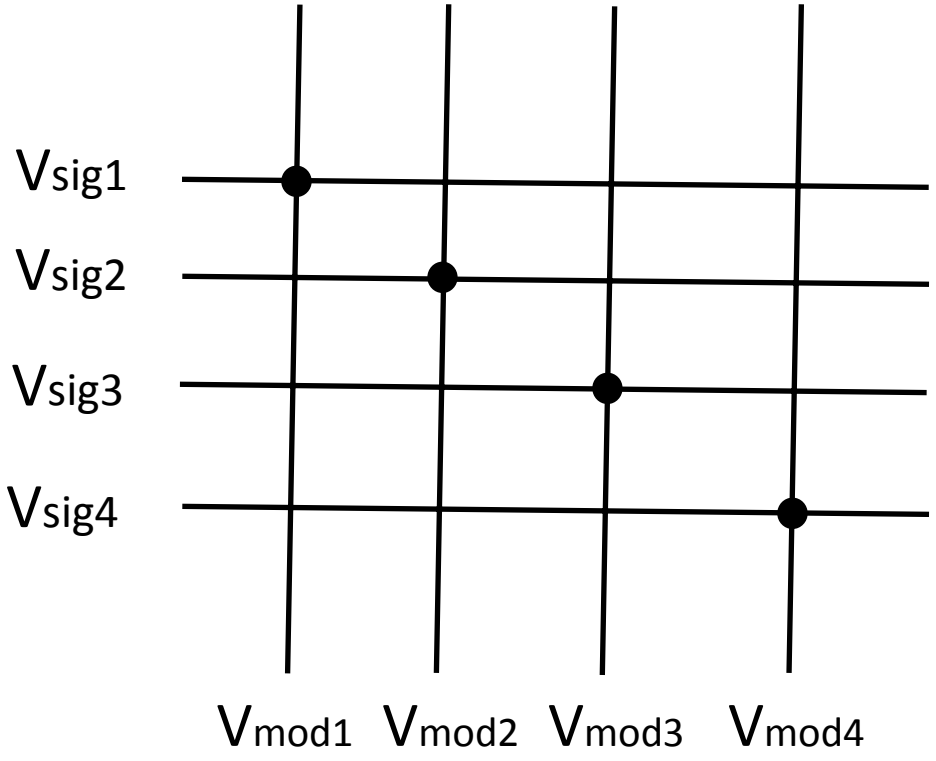
Equivalent circuit at each crossbar junction

$V_{eqB} = V_{inB}\,[(R_i+M_{ij})/(R_i+R_j+M_{ij})]+ V_{inA}[R_j/(R_i+R_j+M_{ij})]$

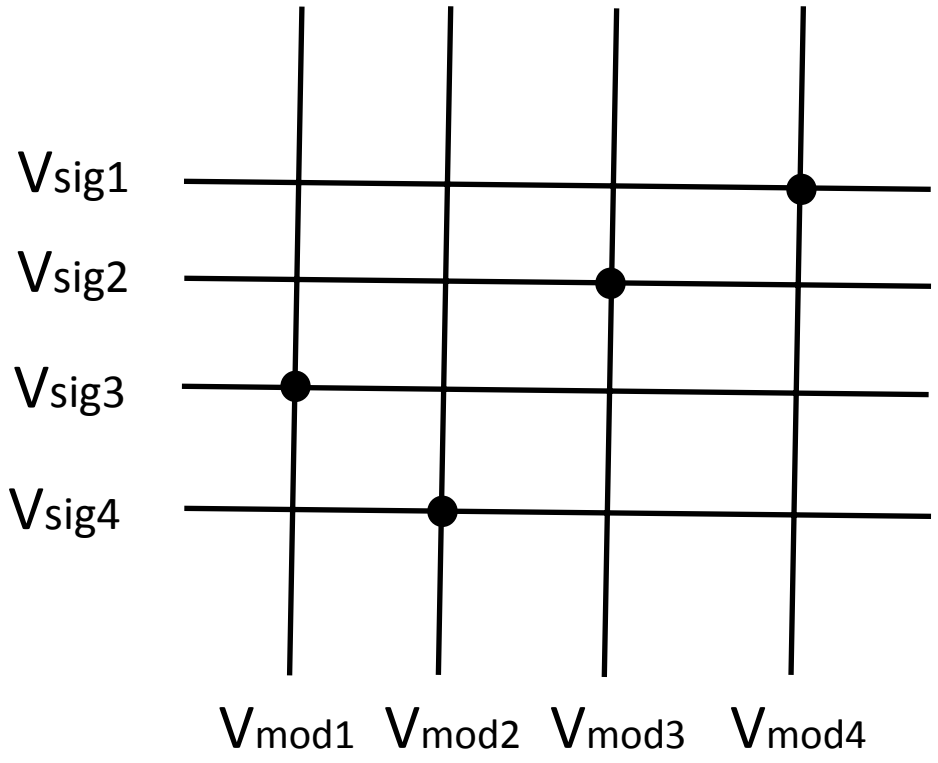
For V_{inB} less than the diode threshold voltage, the resistance state of M_{ij} and voltage state of V_{inA} can be used to modulate signal transmission.



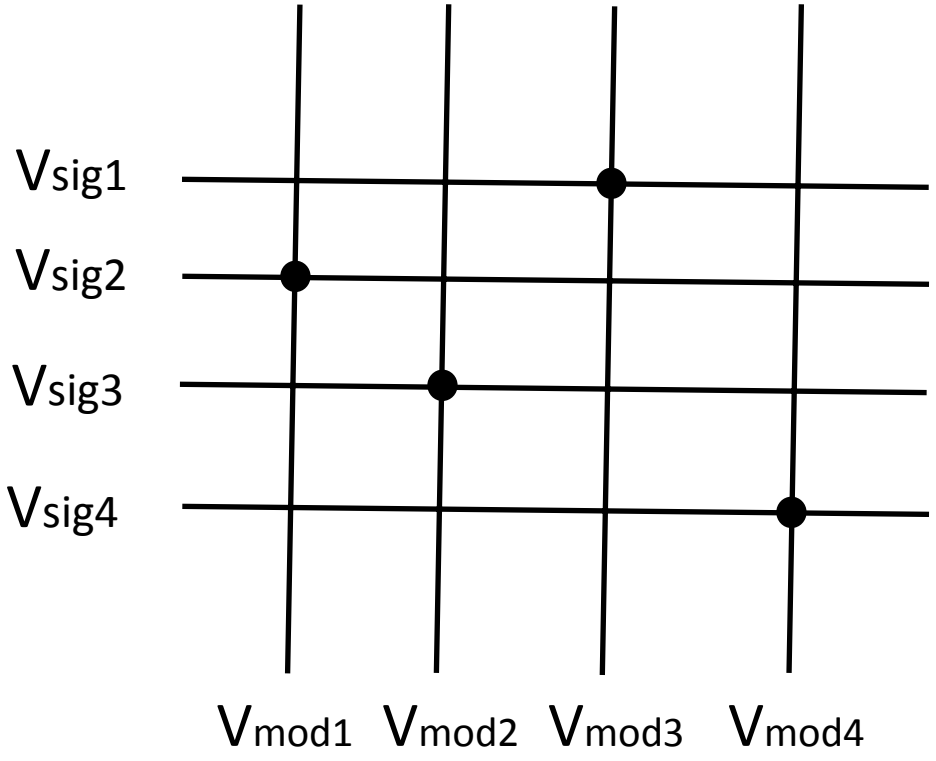
Input Wiring



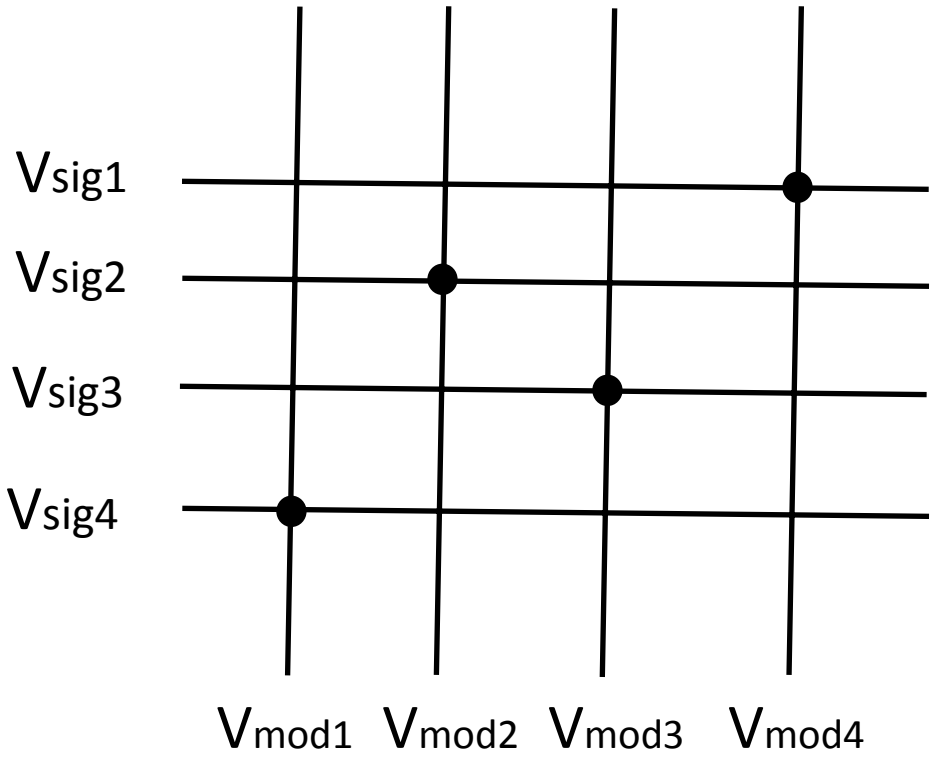
Input Wiring



Input Wiring



Input Wiring



Advantages

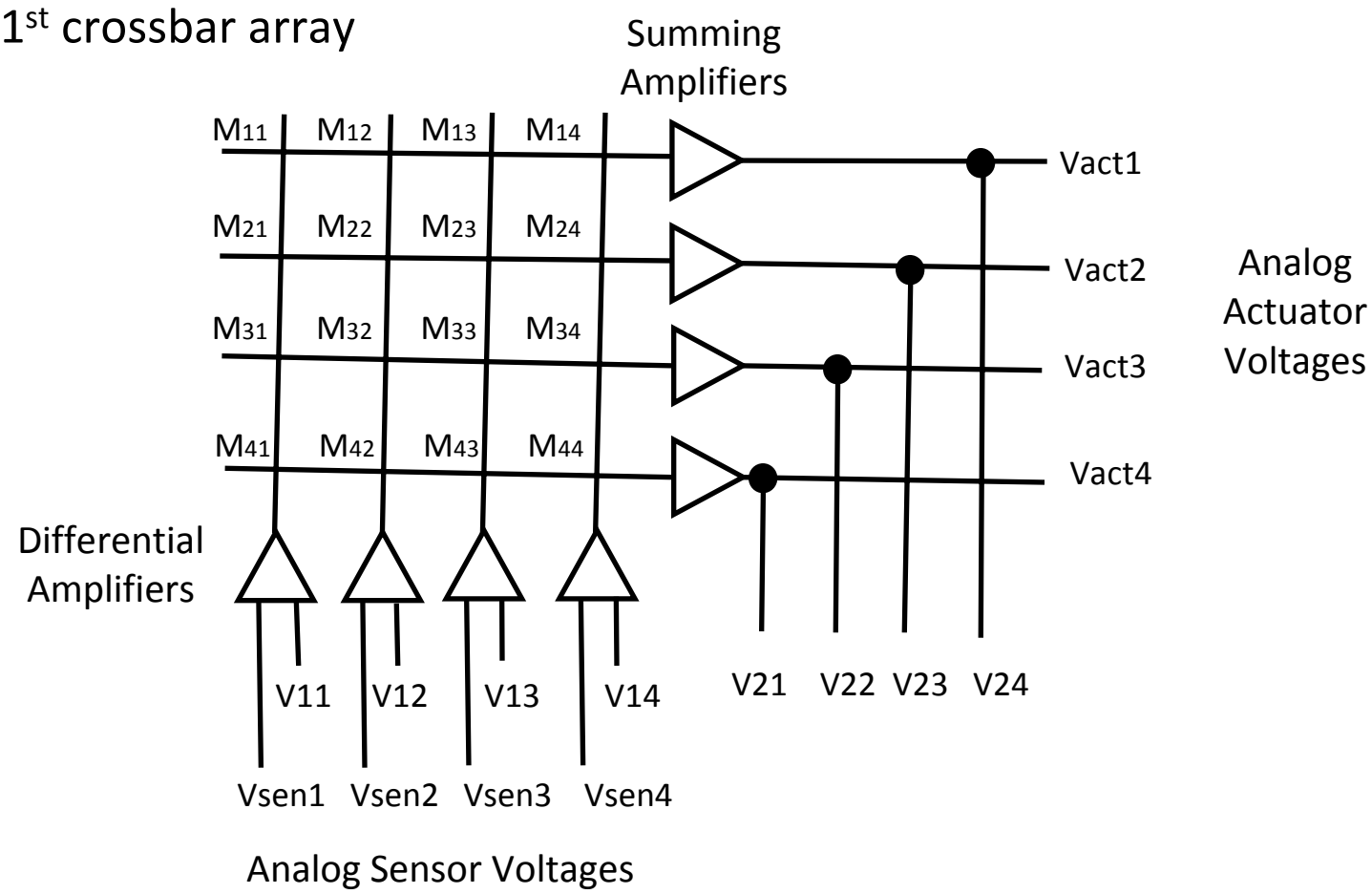
- Switching of carrier frequencies allow more efficient use of spectrum and compensation for crowded channels.
- Potential exist for improved signal encryption by sharing a randomized memristance switching pattern between sender and receiver.

Potential Application #6
Artificial Intelligence

Potential Routes to Strong A.I. with Memristor Crossbars

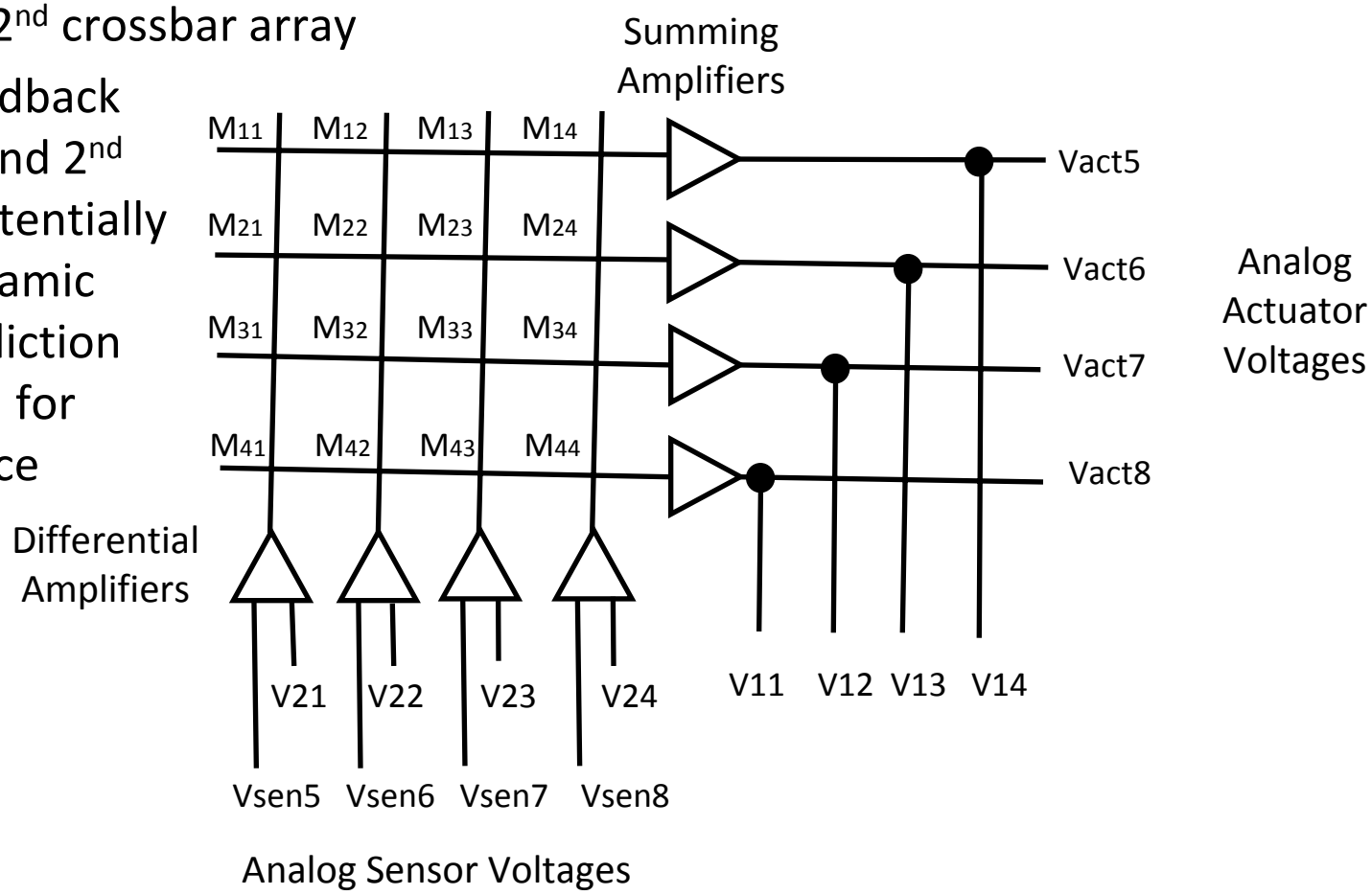
- Neural Networks (feedforward of nonlinear weighted sums of memristance states)
- Genetic Algorithms (selection, crossover, and mutation of memristance states)
- Emergent Complexity from Memory-Prediction Framework (Hawkins approach)

Memristor Crossbar Circuit Design for Sensor Stimulated Emergent Behavior



Memristor Crossbar Circuit Design for Sensor Stimulated Emergent Behavior

Recursive feedback between 1st and 2nd crossbar can potentially set up a dynamic memory-prediction framework for intelligence



Potential Applications #7 and 8
Neural Interfaces (spike counting and classification) and Robotics (enhanced responsiveness for actuator control)

-To be continued at
NSTI Nanotech Conference and Expo
May 3-7, 2009
Houston, TX

Conclusion

- Thank you to organizers and participants.
- Thank you to Dr. Wei Wang of the College of Nanoscale Science and Engineering for information and feedback on FPAAs and suggestion for error analysis.
- Thank you to Jeff Hawkins for insights on memory-prediction framework for intelligence as documented in *On Intelligence*